Research Statement

Rabia Tugce Yazicigil Kirby
Electrical and Computer Engineering (ECE) Department, Boston University (BU)

1 Overview

I lead a collaborative research group at Boston University (BU), where I created the research infrastructure for analog, mixed-signal, and radio frequency (RF) integrated circuit (IC) design. My research is focused on innovating energy-efficient ICs and system solutions in diverse fields, including biosensing, information theory, signal processing, and secure wireless communications. In the past 5.5 years, I've mentored 7 Ph.D. students (1 defended in December 2023), 1 Postdoc (now a Research Scientist at Intel Labs), 7 Masters' students (4 current), and 19 undergraduates (4 current). I am very proud of my team, who are producing high quality results, making an impact in highly interdisciplinary areas, and receiving numerous Fellowships and Awards, such as the *SSCS Predoctoral Achievement Award*, *SSCS Rising Stars*, and several best poster and demo awards, including ISSCC SRP and COMSNETS. I am honored to have received the *2024 NSF CAREER Award*, the *2024 Boston University College of Engineering Excellence in Research Award*, and the *2021 Catalyst Foundation Award*. I am also serving as one of the *SSCS Distinguished Lecturers* for the 2024-2026 term. With funding exceeding $4.85 million from federal, industrial, and philanthropic sources, my lab has published 32 peer-reviewed papers, including contributions to esteemed journals and conferences, such as *Nature*, *JSSC*, and *ISSCC*. It is crucial to highlight that in our field, the publication outlets necessitate the development, fabrication, and experimental testing of a functional chip and integrated system, which is a lengthy process. My research group at BU designed and performed experimental testing of seven chips, while three additional chips are currently being fabricated to demonstrate systems in our three core research areas. Additionally, acceptance of biomedical device research, as outlined in 2.1, requires demonstrating its efficacy in both in vitro and in vivo, underscoring the necessity for a robust and comprehensive integrated system.

2 Specific Research Directions

2.1 Establishing the Field of Cyber-Secure Biological Systems (CSBS)

Funding: NSF (CAREER, SemiSynBio-II), BioMADE/Schmidt Sciences, Helmsley Charitable Trust, Catalyst Foundation, BU CISE Seed/ENG Dean Catalyst Grant, Analog Devices (ADI), Semiconductor Research Corporation (SRC)

Collaborators: MIT: G. Traverso, T. Lu (Now at Senti Bio), BU: D. Densmore, A. Khalil, W. Wong, D. Starobinski, J. Galagan, Industry/Startups: Analog Devices: T. Yu, L. Poo, B. Dufort, Capra BioSciences: A. Magyar, E. Onderko, BioSens8 (Serving as a Scientific Advisor): U. Kuzmanovic

At the core of our scientific methodology, we focus on integrating living sensors—specifically, genetically engineered biological systems—with secure, custom-designed ICs. This fusion defines the nascent field of cyber-secure biological systems (CSBS). By harnessing the power of biology to sense biological phenomena, we unlock the inherent advantages of natural sensors, including robustness in harsh environments, heightened sensitivity, and exceptional specificity. This unique synergy not only taps into the robust attributes of biology but also seamlessly incorporates the reliability and communication infrastructure of electronics. Our CSBS platforms effectively tackle pressing societal challenges in healthcare and environmental monitoring. This scientific approach lays the foundation for transformative advancements, specifically at the convergence of synthetic biology and semiconductor technologies.

2.1.1 Ingestible Bioelectronic Capsules for Gastrointestinal (GI) Diseases: Roughly one in five people endure GI disorders at various stages of their lives. Effective tracking of these inflammatory processes in real time is challenging because the chemical environment in the GI tract is difficult to access and sample. Moreover, many key mediators of inflammatory diseases (e.g., nitric oxide) are extremely short-lived in the body. Profiling these labile (easily broken down) biomolecules that mediate disease and response to medicine would enhance our ability to diagnose, monitor, treat, and prevent GI disorders. The current gold standard for monitoring the GI tract and diagnosing diseases, such as inflammatory bowel disease (IBD), relies on endoscopic biopsies and stool analysis; however, these methods are either invasive (i.e., endoscopic biopsies) or lead to the degradation of valuable labile biomarkers due to non-real-time analysis (i.e., stool analysis). Commercial electronic diagnostic pills, e.g., PillCam, provide a non-invasive and real-time alternative as a powerful technology; however, electronic-only systems are functionally limited since they cannot directly monitor the gut chemical environment. Therefore, to address the major unmet medical need of predicting and preventing IBD, we recently developed a sub-1.4cm^3 ingestible

bio-electronic capsule shown in Fig. 1 detecting critical labile inflammatory biomarkers in situ in real-time [J3, J4, C20].

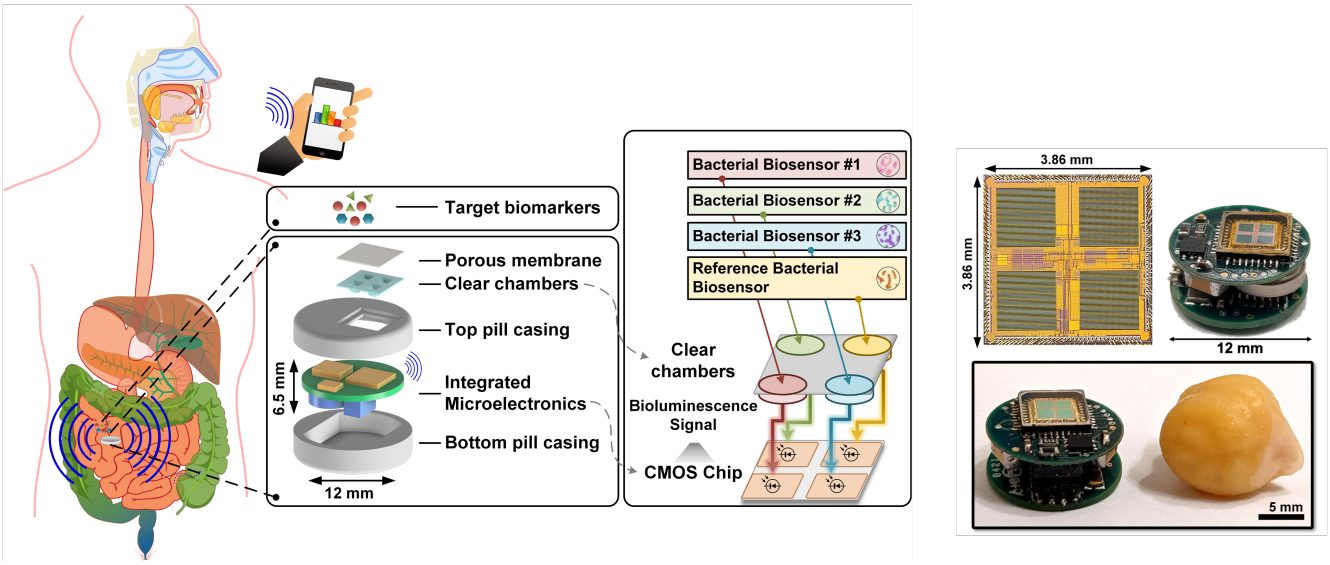

Figure 1: Disease diagnosis and monitoring through synthetic biology and custom CMOS electronics coupling: Our recent work on minimally invasive monitoring of inflammation in the gastrointestinal tract via a miniaturized ingestible bioelectronic capsule [J3, J4, C20]Our miniaturized device leverages the molecular specificity of genetically engineered biological sensors to track these inflammation-associated molecules by producing bioluminescence. Our unique approach converts the weak bioluminescence emitted by these living sensors to a wireless signal using our custom-designed photodetector and low-power electronic readout IC integrated into the device. Our proof-of-concept capsule ($1.35cm^3$) has a form-factor compatible with safe human ingestion and GI transit at 63% size of the commercial state-of-the art (i.e., PillCam; $2.13cm^3$), while consuming only nW-level power ($59nW$) for the custom-designed photodetector and sensor readout IC ($50,000\times$ lower than the state-of-the-art fully integrated solutions). We tested this multi-diagnostic capsule in vitro and in vivo in the GI tract of large animal models (pigs), demonstrating that a human-scale diagnostic device can be built to detect transient mediators of GI inflammatory diseases as a key outcome published in prestigious conferences and journals, CICC'21 [C20], Nature'23 [J3], and JSSC'23 [J4].

Collaboration: My group leads the development of the integrated circuits, design of miniaturized wireless device, and electrical and optical testing. Prof. Giovanni Traverso (MIT MechE) leads packaging and animal studies, and Dr. Timothy Lu (MIT BE / Senti Bio) leads the design of genetically engineered biological sensors.

2.1.2 Hybrid Microfluidic-Bioelectronic Systems: In the quest to efficiently assess and enhance the functionality of biosensors for practical use, traditional experimental methods can be challenging due to their labor-intensive nature. This complexity becomes particularly apparent when dealing with the screening of extensive biosensor libraries, which encompass millions of combinations, across various environmental and chemical variables. Our approach entails the co-design of a modular low-cost droplet microfluidic device seamlessly integrated with embedded CMOS sensors, such as luminescence sensing and impedance spectroscopy as shown in Fig. 2 and as demonstrated at ISSCC SRP'23 [D2 **(Best Poster and Demo Award)**] and ISSCC'24 [C1]. This state-of-the-art innovation transforms the testing process, facilitating swift screening of the biological design space in diverse environments. The outcome is an improved biosensor performance, finely calibrated to specific application conditions, ensuring optimal sensitivity, specificity, and durability.

Lastly, in collaboration with Prof. Douglas Densmore, we are working on a distributed sensor network to achieve cost-effective, real-time, and autonomous wastewater surveillance. This aims to prevent incidents like the Flint water crisis and enable early intervention in unforeseen hazardous conditions resulting from chemicals used in the semiconductor industry or monitoring community illness prevalence.

Collaboration: My group leads the development of the integrated circuits and electrical and optical testing. Prof. Douglas Densmore (BU ECE) leads the design of microfluidics, and Profs. Ahmad Khalil and Wilson Wong (BU BME) lead the design of genetically engineered biological sensors / biological memory.

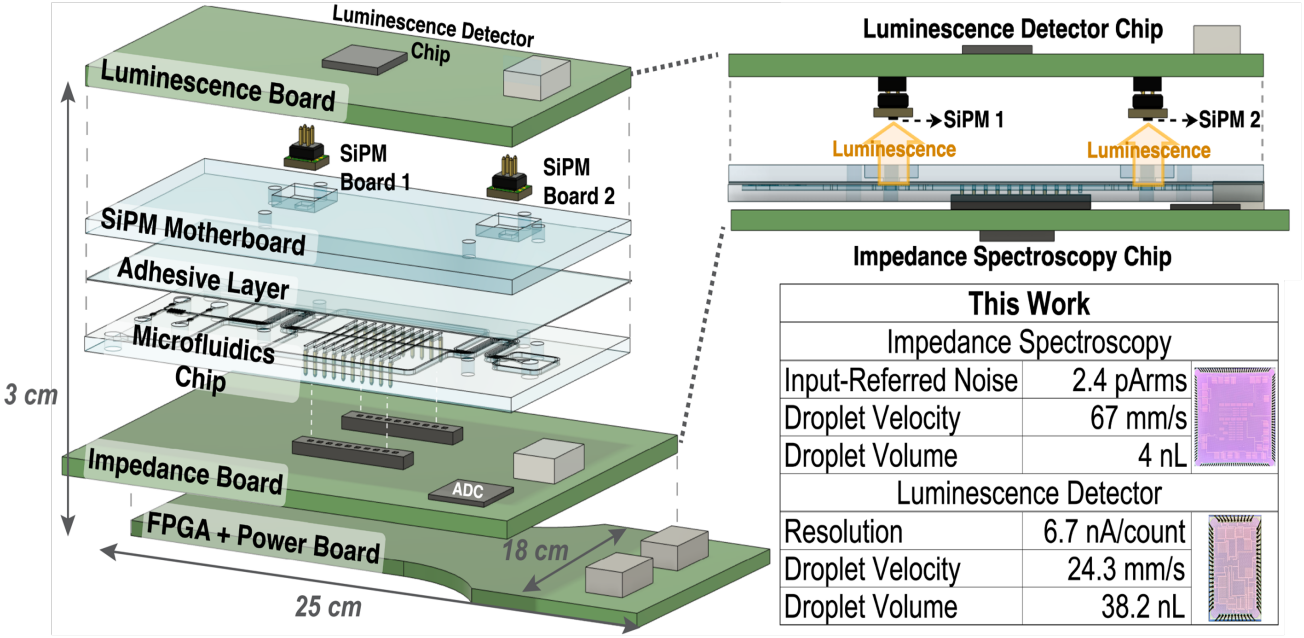

Figure 2: Hybrid platform technology combining droplet microfluidics and custom CMOS electronics for biosensing applications [C1, D2].

2.1.3 Innovating and Expanding CSBS Platforms for Enhanced Biosensing: These custom biosensor IC and system design innovations are at the basis of my NSF CAREER project to *develop the first-of-its-kind secure hybrid bioelectronic sensor technology (CSBS)* for accurate, reliable, and safe real-time in-body monitoring. Given hard resource constraints on energy, computation, and size, securing these devices cannot solely rely on cryptographic mechanisms. My group recently assessed the security vulnerabilities of these resource-constrained wireless systems and analyzed the challenges of embedding security within low-power devices [C10, J1, J5]. Currently, we are developing effective low-power and low-overhead countermeasures leveraging the physical layer. Our work in this area, despite being very new, has gained immediate visibility, and resulted in invited talks at several venues, including Springer Nature Symposium, Brown University, and the California Institute of Technology, and technical tutorials at prestigious conferences, including the IEEE International Solid-State Circuits Conference 2023 [T1].

Developing CSBS platforms not only enable real-world breakthroughs in multi-modal biosensing hardware but also provide a gateway for advancing synthetic biology. This gateway will provide a better understanding of disease mechanisms and management through the development of a multiplexed interfacing platform providing real-time data feedback in situ. This capability will allow disease monitoring and therapeutic planning personalized to each patient while enabling the discovery of disease biomarkers. I have recently established a collaboration with a startup company, BioSens8, as their *Scientific Advisor* to broaden the impact of this sensor technology by custom tailoring it to effectively couple with a novel progesterone biosensor for monitoring fertility health at home. Additionally, my group is designing a CSBS platform for secured continuous monitoring and real-time control of bioreactor technologies for sustainable distributed manufacturing using biology rather than petrochemical sources in collaboration with Capra BioSciences and supported by BioMADE/Schmidt Sciences. My plans include sustained involvement with the DoD's Bioindustrial Manufacturing Innovation Institute (i.e., BIOMADE) for secure biological manufacturing solutions and fostering global collaborations with industry leaders, foundations, and research organizations such as Schmidt Sciences, ADI, SRC, and IMEC.

2.2 All-In-One Data Decoders for Energy-Efficient Wireless Communications

Funding: DARPA, NSF (SWIFT), GlobalFoundries Inc. (GF) Silicon Donation for Chip Fabrication
Collaborators: MIT: M. Medard, Northeastern University: K. Duffy, BU: D. Starobinski

In 1948, Shannon stated that the best error correction performance comes at longer code lengths and in 1978, Berlekamp, McEliece, and Tilborg established that optimally accurate decoding of linear codes is NP-complete in code length so there is no optimally accurate universal decoder at long code lengths. Forward error-correction decoding has traditionally been a code-specific endeavor. Since the design of conventional decoders is tightly coupled

to the code structure, one needs a distinct implementation for each code. The standard co-design paradigm either leads to significantly increased hardware complexity and silicon area to decode various codes or restrictive code standardization to limit hardware footprint. An innovative recent alternative is noise-centric guessing random additive noise decoding (GRAND) shown in Fig. 3. This approach uses modern developments in the analysis of guesswork to create a universal algorithm where the effect of noise is guessed according to statistical knowledge of the noise behavior or through phenomenological observation. Because of the universal nature of GRAND, it allows efficient decoding of a variety of different codes and rates in a single hardware instantiation. The exploration of the use of different codes, including heretofore undecodable ones, e.g., Random Linear Codes (RLCs), is an interesting facet of GRAND. This work enables low-latency, energy-efficient, secure wireless communications in a manner that is future-proof since it will accommodate any type of code. It will allow the United States to leapfrog the state of the art, based on the design of paired codes and decoders, where its historical pre-eminence has frayed.

Collaboration: My group leads the integrated circuit design and electrical testing. Prof. Muriel Medard and Prof. Ken Duffy lead the algorithm development.

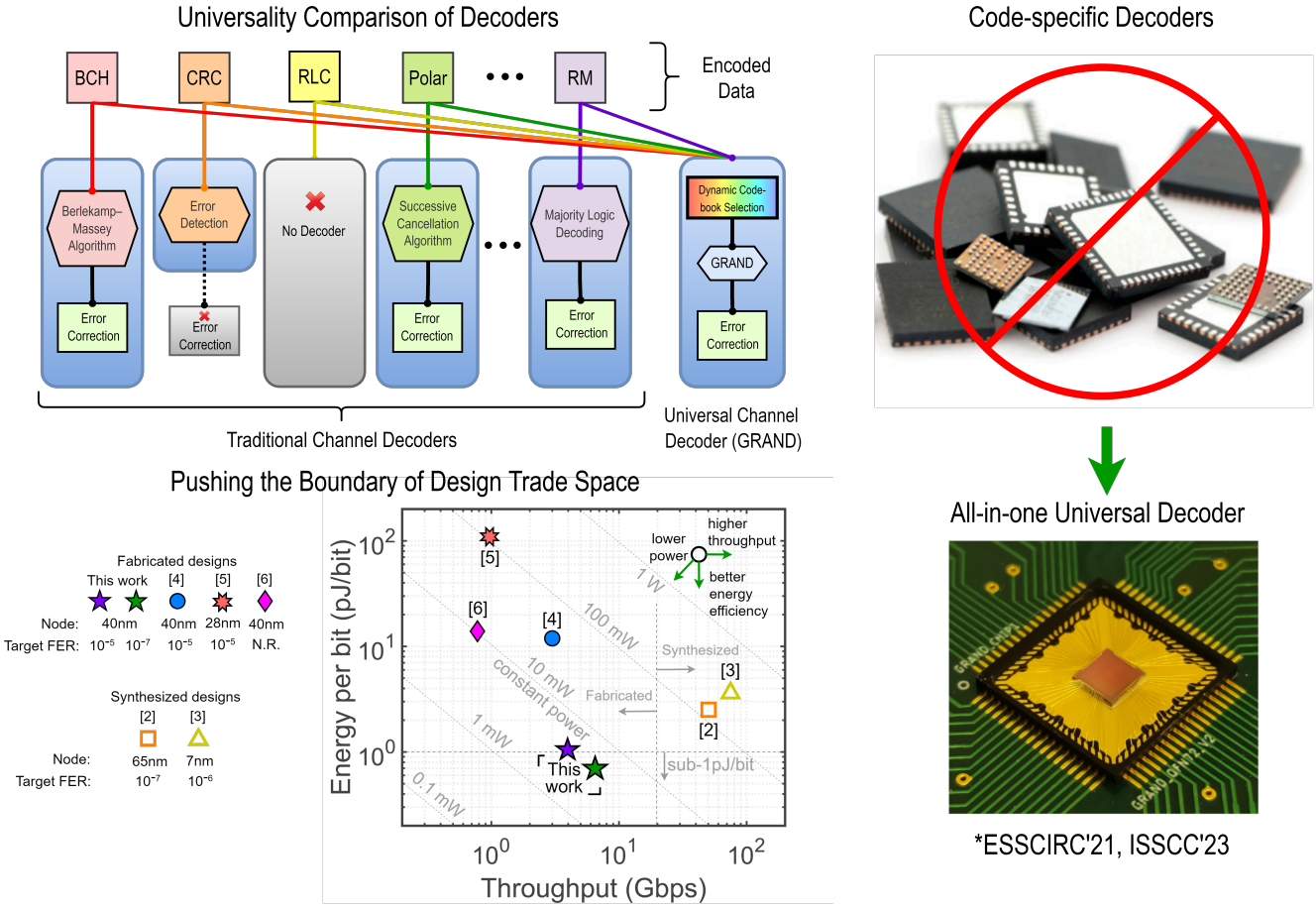

Figure 3: Universal noise-centric decoders achieving lowest energy per bit [C7, C16].

2.2.1 Universal hard-detection decoder (GRAND): My group demonstrated the ***first integrated universal true maximum likelihood (ML) decoder*** at ISSCC SRP'21 [D8], ESSCIRC'21 [C16], 5G WF'21 [D6], COMSNETS'22 [C15 **(Best Research Demo Award)**] targeted for low-power and -latency applications using the GRAND algorithm. This chip has **many firsts**: (1) first to *efficiently decode all binary linear codes of any rate*; (2) first *ML decoding of RLCs*, which are high-performing in theory, but require a universal decoder; (3) first *hard-detection ML decoding of CA-Polar*; (4) first *error correction of up to 3-bit flips for ubiquitous Cyclic-Redundancy-Checks (CRC)s*; (4) first to *provide an additional layer of security through dynamic re-randomization of the code-books* through a code-interleaved architecture. In the pursuit of our research objectives, our focus extends beyond mere chip development. We are actively involved in the creation of comprehensive communication systems centered around the GRAND chip. This all-encompassing approach includes various applications such as

interleaved noise recycling and efficient decoding of product codes. Our successful demonstration of noise recycling, appeared at ICC'22 [C14], FNWF'22 [D4], and COMSNETS'23 [C8 **(Best Demo Award)**], has significantly improved decoding performance by effectively utilizing temporally correlated noise in a single communication channel, while also optimizing energy and latency. Additionally, as an extension of our efforts with the GRAND chip, we demonstrated the efficiency of iterative GRAND (IGRAND) in decoding product codes in our GLOBECOM'21 paper [C17]. This multifaceted approach highlights our dedication to advancing not only chip technology but also the broader landscape of communication systems and decoding methodologies.

2.2.2 Universal soft-detection decoder (ORBGRAND): In our ISSCC'23 paper [C7], my team recently presented the ***inaugural integrated universal soft-detection decoder***, utilizing the ORBGRAND algorithm. This decoder achieved the lowest energy consumption at 0.76pJ/bit and the lowest power consumption at 4.9mW on a small core area and with high throughput performance when compared to state-of-the-art alternatives. The ORBGRAND chip employs soft information from individual received bits to rank order their reliability for assisting the error guessing query order. Significantly, the soft-detection decoder's performance remains unaffected by the code and dynamically enhances its efficiency by reducing energy and latency usage as the conditions of channel noise improve.

We've expanded our earlier interleaved noise recycling method, originally showcased in a hard-detection setting [C14], to include soft-detection decoders utilizing the ORBGRAND chip, as presented in our ISIT'23 paper [C3]. Our team has shown that integrating noise recycling results in a noteworthy decrease in block error rates, along with substantial enhancements in latency and energy efficiency, achieved by reducing the decoding queries. Our innovative approach, involving dynamic lead channel selection for obtaining the initial noise estimate in soft detection scenarios, yields the most significant benefits from noise recycling.

2.2.3 Enhancing the resilience of decoders: The existence of unpredictable jammers, with the ability to overpower transmitted signals, poses a practical obstacle for diverse wireless communication protocols. As a result, wireless receivers need to effectively handle standard channel noise as well as intentional or unintentional jamming. While forward error correction is a common strategy for addressing channel noise, its reliability diminishes when faced with jammers, resulting in a deterioration of error correction performance. In response to this challenge, we have introduced an innovative approach presented in ICC'23 [C4] to enhance the resilience of the recent family of universal error-correcting GRAND algorithms. This method, called Erasure Decoding by Gaussian Elimination (EDGE), specifically impacts the syndrome check block and is applicable to any variant of GRAND. We demonstrate that the EDGE method seamlessly returns to the initial syndrome check function when there are no erasures resulting from jamming. Our simulations have shown that the EDGE variants significantly reduce both the Block Error Rate (BLER) and computational complexity by up to five orders of magnitude compared to the original GRAND and ORBGRAND algorithms under jamming.

Additionally, the impact of bursty jammers is particularly pronounced compared to non-bursty ones, as traditional decoders assume independent noise occurrence for each bit. To overcome this challenge, we proposed a solution that leverages temporal dependencies to identify jammed bits. This involves introducing a pre-decoding step that updates log-likelihood ratio (LLR) reliability information without altering the decoding algorithm. Our method, outlined in GLOBECOM Workshops'22 [C11], significantly enhances decoding performance by accurately identifying a substantial proportion of jamming in received frames. When applied to specific decoding algorithms such as ORBGRAND, our approach reduces the BLER by an order of magnitude for selected codes, effectively preventing a complete denial-of-service scenario at the receiver.

2.3 Energy- and Spectrally Efficient Wireless Systems Embedding Security via Signal-Processing Techniques

Funding: Semiconductor Research Corporation (SRC)
Collaborators: Weizmann Institute of Science: Y. Eldar, Ben-Gurion University of the Negev: N. Shlezinger, MIT: R. Han, A. Chandrakasan, BU: A. Joshi

Conventional radio frequency (RF) systems typically rely on a forceful approach to data acquisition, employing high-resolution quantization and Nyquist sampling rates. This leads to increased power consumption and complexity in hardware design. To overcome these challenges, we demonstrated the incorporation of information-centric (task-specific) algorithms in the creation of adaptable RF receivers (Fig. 4) in our A-SSCC'23 paper [C2]. This strategy seeks to enhance spectrum utilization while minimizing energy consumption, thereby reducing the burden of incorporating security measures at the physical layer.

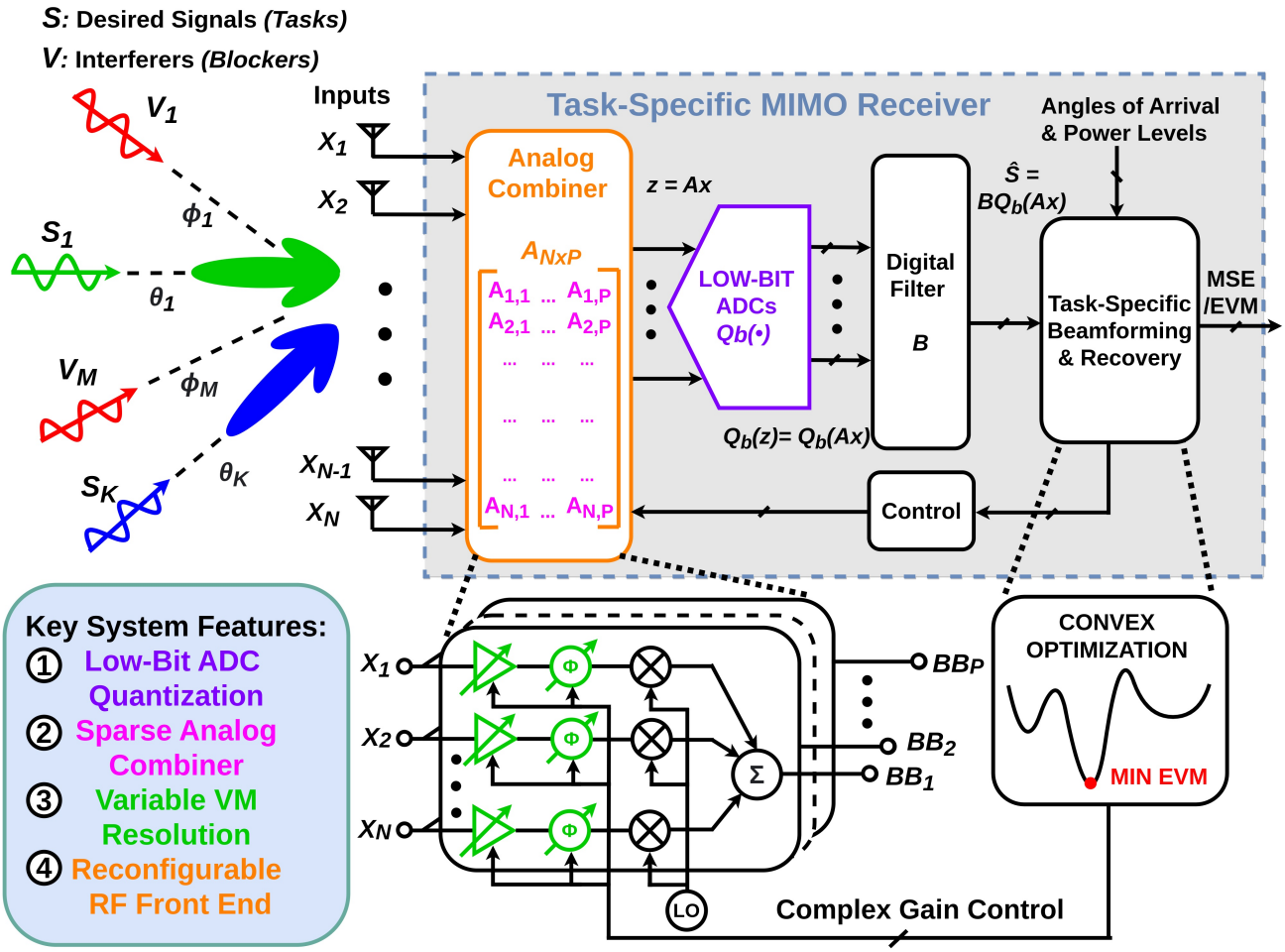

Figure 4: Low-power multiple-input multiple-output (MIMO) receiver leveraging task-specific beamforming [C2, C13, M1, Pre3, B1].

Addressing security concerns at the physical-layer-design level is crucial, rather than treating them as an afterthought in software or digital algorithms, especially in the context of future sensing and communication systems. The physical layer's attack surface can be exploited through side-channel attacks and manipulation of fundamental RF/analog signal and channel parameters. To establish secure analog/RF circuits and wireless sensing systems, it is imperative to comprehend and scrutinize these vulnerabilities using universal metrics. Efforts to mitigate these vulnerabilities entail the development of hardware-algorithmic techniques that capitalize on the distinctive characteristics of the physical layer and integrated circuit components for security. The selection of suitable security protocols and RF/analog security primitives necessitates a systematic examination of performance trade-offs, considering factors such as energy consumption, latency, and area implications, particularly in tightly resource-constrained systems.

Our collaborative research in this area is laying the key foundations for physical-layer security in energy-efficient wireless communications, computation, and sensing as discussed in OJ-SSCS'23 [J1] and SSCM'20 [M2] and includes: Ultra-fast bit-level frequency hopping with physical-layer encryption: RFIC'18 [C24], SSCM'20 [M2]; Miniaturized THz package-less cryptographic tags: ISSCC'20 [C22], JSSC'21 [J8]; Dual-factor authentication of medical implants: CICC'20, CBMS'21 [C21, C18]; Secure compressed-sampling spectrum sensing: DySPAN'19 [C23]; Physical-layer security for wireless with OAM: RFIC'21 - **best student paper award** [C19], JSSC'22 [J6], SipS'22 [C12]; Secure phase-based ranging systems for IoT: ACM JETC'22 [J5]; Security of ingestible devices: BioCAS'22 [C10]; Soft-information decoding security against smart bursty jammers: GLOBECOM'22 Workshops [C11]; Jamming-resilient universal error-and-erasure decoding: ICC'23 [C4]; Bootstrappable Homomorphic Encryption: HPCA'23 [C9]; Secure THz wake-up receivers CICC'23 – **best student paper candidate** [C6], JSSC'24 [J2]. Furthermore, I delivered tutorials on IoT security at the international cyber security event Cyber Week 2019 and a technical tutorial focusing on physical-layer security for energy- and latency-constrained integrated systems at the IEEE International Solid-State Circuits Conference 2023 [T1].

Publications, Demos, and Tutorials

The names of advised students/postdocs at Boston University are underlined. The names of co-advised/co-mentored students at MIT and Columbia University are indicated with *.

- Total number of peer-reviewed publications: 42
- Google Scholar Link: `https://scholar.google.com/citations?user=kWZ-qQQAAAAJ&hl=en&oi=ao`
- Total number of citations (Google Scholar, April 7, 2024): 705
- H-index (Google Scholar, April 7, 2024): 16

Book Chapters [B]

1. D. Malak, **R. T. Yazicigil**, M. Medard, X. Zhang, and Y. Eldar, *Women in Telecommunications: Task-Based Quantization in Systems*, Women in Engineering and Science, Springer Books, October 2023.

Magazine Articles [M]

1. S. Mulleti, T. Zirtiloglu, A. Tan, **R. T. Yazicigil**, Y. Eldar, *Power-Efficient Sampling*, under review, **Feature Article** in IEEE Signal Processing Magazine, 2023.
2. **R. T. Yazicigil** et al., *Beyond Crypto: Physical-Layer Security for Internet of Things Devices*, **Invited Feature Article**, IEEE Solid-State Circuits Magazine, vol. 12, no. 4, pp. 66-78, Fall 2020.
3. **R. T. Yazicigil**, T. Haque, P. R. Kinget, and J. Wright, *Taking Compressive Sensing to the Hardware Level: Breaking Fundamental Radio-Frequency Hardware Performance Tradeoffs*, **Feature Article** in IEEE Signal Processing Magazine, vol. 36, no. 2, pp. 81-100, March 2019.

Journal Articles [J]

1. A. Yasar, **R. T. Yazicigil**, *Physical-Layer Security for Latency- and Energy-Constrained Integrated Systems*, **Invited for a Submission** in IEEE Open Journal of the Solid-State Circuits Society, vol. 3, pp. 262-273, 2023.
2. E. Lee*, M. I. W. Khan, X. Chen, U. Banerjee, N. Monroe, **R. T. Yazicigil**, R. Han, and A. P. Chandrakasan, *A 1.54-mm^2, 264-GHz Wake-Up Receiver With Integrated Cryptographic Authentication for Ultra-Miniaturized Platforms*, **Invited for a Submission** in IEEE Journal of Solid-State Circuits, vol. 59, no. 3, pp. 653-667, March 2024.
3. M. E. Inda, M. Jimenez, Q. Liu, N. Phan, J. Ahn, C. Steiger, A. Wentworh, A. Riaz, T. Zirtiloglu, K. Wong, K. Ishida, N. Fabian, J. Jenkins, J. Kuosmanen, W. Madani, R. McNally, Y. Lai, A. Hayward, M. Mimee, P. Nadeau, A. Chandrakasan, G. Traverso$^+$, **R. T. Yazicigil**$^+$, T. K. Lu$^+$, *Sub-1.4 cm^3 Capsule for Detecting Labile Inflammatory Biomarkers In Situ*, **Nature** 620, 386–392, 2023. $^+$= Co-corresponding authors.
4. Q. Liu, M. Jimenez, M. E. Inda, A. Riaz, T. Zirtiloglu, A. Chandrakasan, T. K. Lu, G. Traverso, P. Nadeau, and **R. T. Yazicigil**, *A Threshold-based Bioluminescence Detector with a CMOS-Integrated Photodiode Array in 65nm for a Multi-Diagnostic Ingestible Capsule*, in IEEE Journal of Solid-State Circuits, vol. 58, no. 3, pp. 838-851, March 2023.
5. A. Riaz, D. Nash, J. Ngo, C. Juvekar, P. Nadeau, T. Yu, and **R. T. Yazicigil**, *Security Assessment of Phase-Based Ranging Systems in a Multipath Environment* in ACM Journal on Emerging Technologies in Computing Systems, Special Issue on Secure Radio-frequency (RF)-Analog Electronics and Electromagnetics, vol. 18, issue 4, article no.: 66, pp. 1–19, October 2022.
6. M. I. W. Khan, J. Woo*, X. Yi, M. I. Ibrahim, **R. T. Yazicigil**, A. P. Chandrakasan, and R. Han, *A 0.31-THz Orbital-Angular-Momentum (OAM) Wave Transceiver in CMOS with Bit-to-OAM Mode Mapping*, **Invited for a Submission** for the RFIC 2021 Special Issue in IEEE Journal of Solid-State Circuits, vol. 57, no. 5, pp. 1344-1357, May 2022.

7. X. Yi, C. Wang, Z. Hu, J. Holloway, M. I. W. Khan, M. I. Ibrahim, M. Kim, G. C. Dogiamis, B. Perkins, M. Kaynak, **R. T. Yazicigil**, A. P. Chandrakasan, and R. Han, *Emerging Terahertz Integrated Systems in Silicon*, **Invited feature article** in IEEE Transactions on Circuits and Systems I, vol. 68, no. 9, pp. 3537-3550, September 2021.

8. M. I. Ibrahim, M. I. W. Khan, C. S. Juvekar, W. Jung, **R. T. Yazicigil**, A. P. Chandrakasan, and R. Han, *CMOS THz-ID: A 1.6mm^2 Package-Less Identification Tag Using Asymmetric Cryptography and 260-GHz Far-Field Backscatter Communication* in IEEE Journal of Solid-State Circuits, vol. 56, no. 2, pp. 340-354, February 2021.

9. **R. T. Yazicigil**, T. Haque, M. Kumar*, J. Yuan*, J. Wright, and P. R. Kinget, *How to Make Analog-to-Information Converters Work in Dynamic Spectrum Environments With Changing Sparsity Conditions* in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 65, no. 6, pp. 1775-1784, June 2018.

10. **R. T. Yazicigil**, T. Haque, M. R. Whalen*, J. Yuan*, J. Wright, and P. R. Kinget, *Wideband Rapid Interferer Detector Exploiting Compressed Sampling With a Quadrature Analog-to-Information Converter*, **Invited for a Submission** for the ISSCC 2015 Special Issue in IEEE Journal of Solid-State Circuits, vol. 50, no. 12, pp. 3047-3064, December 2015.

11. T. Haque, **R. T. Yazicigil**, K. J. Pan, J. Wright, and P. R. Kinget, *Theory and Design of a Quadrature Analog-to-Information Converter for Energy-Efficient Wideband Spectrum Sensing* in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 62, no. 2, pp. 527-535, February 2015.

Conference Papers (Peer-reviewed) [C]

1. Q. Liu, D. Arguijo Mendoza, A. Yasar, D. Caygara, Aya Kassem, D. Densmore, and **R. T. Yazicigil**, *Droplet Microfluidics Co-Designed with Real-Time CMOS Luminescence Sensing and Impedance Spectroscopy of 4nL Droplets at a 67mm/s Velocity*, **with a Live Hardware Demonstration**, IEEE International Solid-State Circuits Conference (ISSCC), San Franscisco, CA, USA, 2024.

2. T. Zirtiloglu, P. Crary, E. Tasci, Y. Eldar, N. Shlezinger, and **R. T. Yazicigil**, *Task-Specific Beamforming MIMO Receiver Using 2-Bit Analog-to-Digital Converters*, IEEE Asian Solid-State Circuits Conference (A-SSCC), Haikou, China, pp. 1-3, 2023.

3. Z. E. Kizilates, A. Riaz, G. F. Coraluppi, M. Medard, K. Duffy, and **R. T. Yazicigil**, *Leveraging Noise Recycling in Soft Detection Decoding Using ORBGRAND*, **invited**, Special Session: IEEE International Symposium on Information Theory (ISIT), Taipei, Taiwan, pp. 1085-1089, 2023.

4. F. Ercan, K. Galligan, D. Starobinski, M. Medard, K. Duffy, and **R. T. Yazicigil**, *GRAND-EDGE: A Universal, Jamming-resilient Algorithm with Error-and-Erasure Decoding*, 2023 IEEE International Conference on Communications (ICC), Rome, Italy, pp. 4501-4507, 2023.

5. A. Riaz, Z. E. Kizilates, A. Yasar, F. Ercan, W. An, J. Ngo, K. Galligan, M. Medard, K. Duffy, and **R. T. Yazicigil**, *Demo: Universal Soft-Detection Decoder with Ultra-Low Energy Consumption Using ORB-GRAND*, IEEE 24th International Symposium on a World of Wireless, Mobile and Multimedia Networks (WoWMoM), Boston, MA, USA, pp. 337-339, 2023.

6. E. Lee*, M. I. W. Khan, X. Chen, U. Banerjee, N. Monroe, **R. T. Yazicigil**, R. Han, and A. P. Chandrakasan, *A 1.54 mm^2 Wake-up Receiver Based on THz Carrier Wave and Integrated Cryptography Authentication*, **Best Student Paper Candidate**, 2023 IEEE Custom Integrated Circuits Conference (CICC), San Antonio, TX, USA, pp. 1-2, 2023.

7. A. Riaz, A. Yasar,F. Ercan, W. An, J. Ngo, K. Galligan, M. Medard, K. Duffy, and **R. T. Yazicigil**, *A Sub-0.8pJ/b 16.3Gbps/mm^2 Universal Soft-Detection Decoder Using ORBGRAND in 40nm CMOS*, **with a Live Hardware Demonstration**, IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, pp. 432-434, 2023.

8. A. Riaz, A. Solomon, F. Ercan, M. Medard, **R. T. Yazicigil**, and K. R. Duffy, *Noise Recycling using GRAND for Improving the Decoding Performance,* **Best Demo Award**, 15th International Conference on COMmunication Systems & NETworkS (COMSNETS), Bangalore, India, pp. 171-173, 2023.

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