Chapter 18
Dimming and Modulation for VLC-Enabled Lighting

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Abstract Advances in high brightness light emitting diode (LED) technology are enabling myriad applications in lighting including visible light communications (VLC) technology that has the potential to complement RF technology to provide wireless data access for indoor coverage. This chapter reviews various dimming techniques suitable for VLC, and presents an LED driver circuit architecture incorporating digitally controlled analog circuit blocks to deliver concurrent dimming control and data transmission for VLC-enabled lighting. To achieve this target, a bi-level pulse-width modulation (PWM) driving scheme is applied to enable data transmission during the "off" period of the LED drive current while concurrently providing dimming control. The proposed architecture is compatible with digital baseband modulation schemes and implements a mechanism for ease of integration with commercial off-the-shelf (COTS) LED drivers for VLC system realization. This chapter also discusses a dimming compatible analog baseband modulation scheme. The reverse polarity optical orthogonal frequency-division multiplexing (RPO-OFDM) is a recent approach to realize compatibility between any format of an analog OFDM signal suitable for optical transmission and the

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concept of a digital pulse-width modulation (PWM) technique for dimming control. We also describe an implementation of the RPO-OFDM approach as part of a wireless access testbed. Experiments reveal that bit-error and bit-rate performances are maintained over a wide range of dimming.

Keywords Analog dimming · Data-dimming multiplication · Dimming control · Light emitting diode (LED) · LED driver · Orthogonal frequency-division multiplexing (OFDM) · Pulse position modulation (PPM) · Pulse-width modulation (PWM) · Reverse polarity optical OFDM(RO-OFDM) · Visible light communications (VLC)

18.1 Introduction

The global quest towards energy efficiency in lighting via solid-state devices opens new possibilities for architectural lighting systems, consisting of networked solid-state lamps with multi-variable distributed control, adaptive features to alter color quality and temperature, and high-speed data transmission. The emergence of non-traditional, disruptive illumination applications for light emitting diodes (LEDs) introduces new challenges in the development of driver circuits. For visible light communications (VLC) driver circuit, compatibility with standard pulse-width modulation (PWM) dimming control methods plays a crucial role [1]. The faster modulation capability of LED devices relative to other light sources has produced considerable interest in the use of solid-state illumination systems for data communication. Achieving this goal is not possible without an optical transmitter that has the capability of transmitting data while providing and maintaining user-defined brightness control. Low-power CMOS technology enables realization of system-on-chip driver circuits integrating multiple functions to control LED device performance, luminance, and data modulation for "intelligent" visible light networking. This chapter presents multilevel digital and analog modulation schemes for implementation in LED driver designs suitable for data transmission and dimmable illumination control [2–4]. An LED driver circuit architecture is presented that incorporates analog and digital circuit blocks to deliver concurrent dimming control and data transmission. This is achieved by independent control of output voltage and current using buck converter and current control loops, respectively. This integrated system incorporates the feedback mechanisms to provide uniform light output together with the peak current control, which also prevents flickering. The proposed architecture is flexible enough to take any digital baseband modulation format. Designed and implemented in a 180 nm CMOS process, it provides linear 10–90 % dimming control while transmitting data. On the other hand, we can achieve distinct advantages using the advanced multi-carrier modulation techniques such as orthogonal frequency-division multiplexing (OFDM). The spectral efficiency of OFDM is capable of overcoming the limited modulation bandwidth of LEDs. The reverse polarity optical OFDM (RPO-OFDM) is an approach to realize compatibility

between any format of an analog OFDM signal suitable for optical transmission and the concept of a digital PWM technique for dimming control. The basic idea is superimposing the OFDM signal on top of a PWM dimming signal. The experimentally obtained measurements of wireless access testbed demonstrate linear wide-range dimming while maintaining both bit-error and bit-rate performances.

18.2 Digital Modulation with Dimming Concepts

In the design of LED drivers for VLC applications, it is necessary to control the output luminous intensity of an LED while transmitting data. LEDs are current-driven devices and the luminous intensity of an LED is typically controlled by its forward current. The peak emission wavelength of LEDs tends to shift with variations in forward current, which can lead to color variations at different dimming levels. This effect does not make the amplitude-mode (DC) dimming method always suitable for VLC applications. PWM dimming schemes, in contrast, provide illumination control by generating a current pulse train with varying duty cycle yield the same average drive current as achieved using the analog technique. With better chromaticity control and linear dimming capability, the PWM dimming technique is preferred where dimming is required at the expense of degradation in luminous efficiency [5, 6]. In addition to dimming, an LED driver for VLC-enabled lighting supports data modulation. The combination of PWM and modulation depth variation can be used for concurrent brightness control and data communication. Variable pulse position modulation (VPPM) is a commonly used approach; VPPM symbols are determined by their positions and for dimming purposes the duty cycle of each symbol will be modified accordingly [7]. The IEEE 802.15.7 standard for short-range wireless optical communication using visible light outlines several modulation schemes, including variable on–off keying (VOOK) and VPPM schemes for light dimming [8]. A study of dimming mechanisms with the capability of being implemented in VLC systems optimized for energy efficiency and providing illumination control is reported in [9]. A multilevel modulation scheme featuring data transmission and dimming control is presented in [10] by combining PAPM (pulse amplitude position modulation) with PWM, which is referred to as variable pulse amplitude and position modulation (VPAPM). The power and bandwidth efficiency of this scheme are calculated and compared to other modulation schemes such as return-to-zero OOK (RZ-OOK), VOOK, and VPPM. This VPAPM scheme has higher bandwidth efficiency compared to other schemes. There are several reports of dimming techniques combined with PPM modulation schemes. A multiple PPM (MPPM) is proposed in [11] to generate a modulated data stream with concurrent brightness control. Based on the dimming level, the number of optical MPPM pulses is controlled within one symbol duration. MPPM schemes can achieve a higher spectral efficiency with less optical power when compared to VOOK and VPPM. Expurgated PPM (EPPM) is proposed in [12] for indoor VLC dimming applications, providing a wide range of peak-to-average

power ratios (PAPR). At the receiver, a correlation decoder is employed that is optimal for shot noise and background-light limited systems. In addition, an interleaving method is implemented, which improves the performance of EPPM schemes compared to PPM for VLC systems or any other dispersive optical wireless communication (OWC) system. This advantage is based on the ability to reduce inter-symbol interference (ISI) and further decrease of error probability. An overlapped EPPM pulse technique is proposed to increase the transmission rate when bandwidth-limited white LEDs are used [12]. One implementation of VPPM is reported in [13], where a dual-purpose offline LED driver with illumination control and data communication is designed. The proposed dual-purpose offline LED driver utilized the average current mode control to realize a constant current source using a buck converter without a capacitor. The VLC link is implemented using a shunt switch in parallel with LED string controlled by the VPPM as the data stream. An experimental demonstration of concurrent brightness control with data transmission for a VLC system is presented in [14]. A PWM scheme is adopted for LED brightness control and a combined PPM-PWM scheme generates a modulated data stream. To maintain independent control of light dimming while transmitting data, the PWM dimming period is set as an integer multiple of the PPM slot duration. The LEDs are modulated by the PPM–PWM signal and the recovered eye diagrams prove the independent dimming control during the data transmission for a range of dimming levels. Several LED driver circuit architectures are described in the following sections to enable realization of both analog and digital techniques for concurrent data transmission and dimming control.

18.3 Digital Techniques

This section presents the building block and operation of digitally controlled LED driver to deliver simultaneous illumination control and serial data transmission. To achieve this goal, a bi-level PWM driving scheme is applied to enable data transmission during the "off" period of the LED drive current. With 3-bit PWM dimming resolution, the driver circuit enables linear luminous intensity control from 5 to 100 %. Pseudo-random binary sequences (PRBS) are generated to compare circuit performance for various data modulation formats. The LED driver circuit exhibits a worst-case power consumption of 100 mW with 33 mA of peak PWM current. The LED driver circuit architecture depicted in Fig. 18.1 performs concurrent illumination control and data transmission based on a 3-bit PWM digital control signal. Uninterrupted serial data transmission is enabled during the PWM off-time by implementing a bi-level drive current scheme [2].

Figure 18.1 shows the schematic of the proposed design, which is composed of digital and analog circuit blocks. The circuit is controlled by a 3-bit PWM dimming control signal (B_0, B_1, and B_2), which sets the degree of brightness. The PWM symbol "001" corresponds to the lowest illumination level and symbol "111" corresponds to maximum brightness. The digital timing circuit block generates

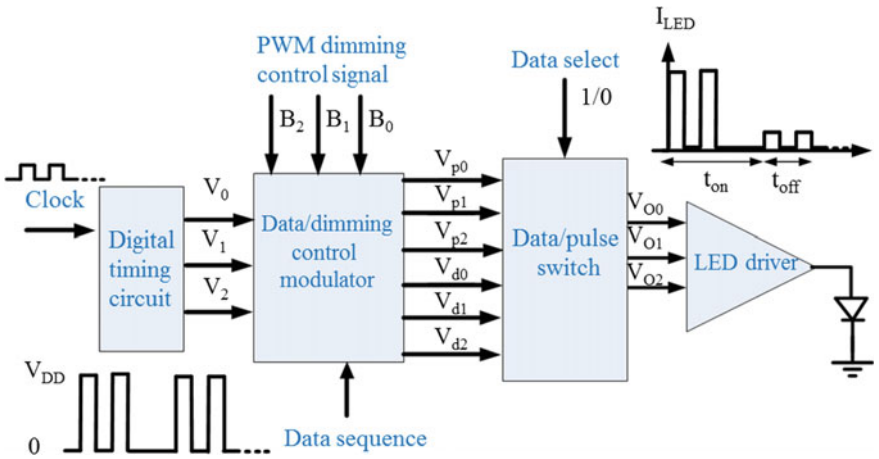

Fig. 18.1 A digitally controlled LED driver circuit block diagram

three reference pulse waveforms (V_0, V_1, and V_2) to enable 8 levels of PWM modulation based on the input clock signal frequency. The data/dimming control modulator circuit block generates voltage waveforms combining a modulated data sequence with the PWM dimming control signal. This circuit block also generates a scaled data sequence during the PWM pulse off-times (t_{off}) in order to enable uninterrupted data transmission. The digital timing circuit and data/dimming control modulator circuit are both digital blocks, composed of logic gates, switches, buffers, and delay circuits. The outputs of the data/dimming control modulator circuit are divided into two different groups of waveforms based on the presence of an input serial data sequence. The first group (V_{d0}, V_{d1}, and V_{d2}) is a set of dimming waveforms generated when the "data select" signal is enabled; and the second group (V_{p0}, V_{p1}, and V_{p2}) for "data select" disabled. The output signals from the data/pulse switch (V_{o0}, V_{o1}, and V_{o2}) circuit block drive an analog LED driver stage, which generates variable current pulses to control the LED average forward current. This digital unit generates three distinct digital reference pulse waveforms (V_0, V_1,

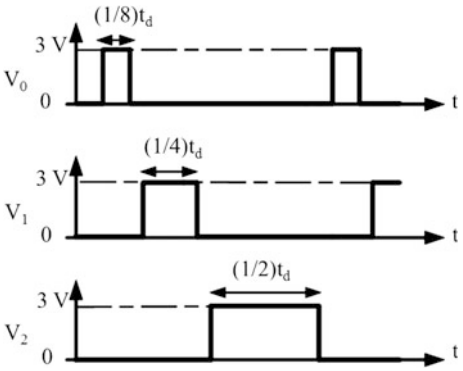

Fig. 18.2 Output waveforms of the digital timing circuit

and V_2) with different duty ratios based on the 3-bit PWM dimming control signal (B_0, B_1, B_2) as shown in Fig. 18.2. These three waveforms are generated using the delay and XOR digitals blocks. The period of the reference clock signal is t_d.

18.3.1 Data/Dimming Control Modulator

Figure 18.3 presents the data/dimming control modulator circuit. This circuit block is composed of logic circuits and CMOS switches as shown in Fig. 18.3a. The schematic view of a single branch is shown in Fig. 18.3b. Signal B_x represents the 3-bit PWM control signal (B_0, B_1, and B_2), where V_x, V_{dx}, and V_{px} are signal waveforms corresponding to input and output signals for each identical branch of the circuit. A dimming switch is implemented using the parallel combination of NMOS and PMOS transistors, where two resistors are used to pass data during the PWM off-time period. The logic unit is composed of AND and NAND gates. The AND gate generates PWM waveforms based on the PWM control bits. The AND gate generates a logic zero if the control bit is low, and passes signal V_x to the output if the control bit is set high. Thus, PWM signals corresponding to the predefined values of B_0, B_1, and B_2 will appear at the output of the AND gate. To generate a PWM waveform combining modulated data, the circuit generates a scaled version of the input data sequence using a resistor-divider network, as shown in Fig. 18.3b. The NAND gate enables a scaled version of the input data sequence to pass through the switch during the PWM off-time period. The resistors are implemented using gate-controlled transistors operating in linear mode, enabling variable control of the scaled data voltage amplitude.

The resulting drive signal waveform consists of the data pulses with maximum amplitude during the PWM on-time and scaled amplitudes during the off-time. The scaled amplitudes are set to achieve an adequate signal level to drive the final analog driver stage.

The minimum signal amplitude is a function of the threshold voltage of the input transistor in the following stage. The data/pulse switch circuit shown in Fig. 18.1 is composed of three switches. This unit will pass V_{dx} waveforms to the output only if the data select signal is set high. The final stage is an analog LED driver circuit

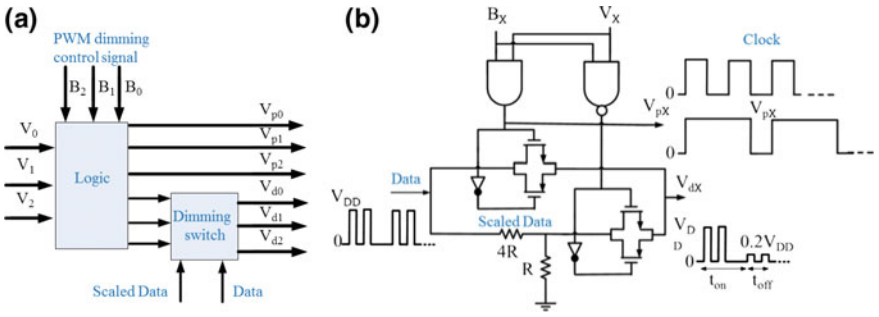

Fig. 18.3 Data/dimming control modulator circuit for digital dimming

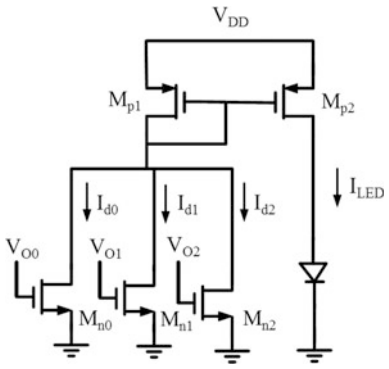

Fig. 18.4 Analog circuit schematic of digitally controlled LED driver

composed of three identical NMOS transistors (M_{n0}, M_{n1}, and M_{n2}) and a current mirror circuit (M_{P1} and M_{P2}), as in Fig. 18.4.

The NMOS transistors generate current waveforms (I_{d0}, I_{d1}, I_{d2}) proportional to the voltage waveforms V_{o0}, V_{o1}, and V_{o2}, produced by the data/dimming control modulator circuit. The peak current of 33 mA is pumped into the LED. The three parallel current waveforms are summed at the transistor drain node and mirrored to form the LED forward current. The resulting LED current waveform is linearly proportional to sum of the driving voltage waveforms. At dimming levels close to 0 %, the data transmission will degrade significantly. One way to alleviate this problem is uninterrupted data transmission as explained further in this chapter. However, the lowest dimming level is set based on the receiver sensitivity and link range.

18.4 Circuit Architecture

This section presents the LED driver circuit architecture to deliver concurrent dimming control and data transmission. This is achieved by independent control of output voltage and current using buck converter and current control loops, respectively. This is a design that can be applied to transform off-the-shelf LED drivers into optical transmitter circuits for VLC applications. It also has the capability of sending data signals in the format of non-return-to-zero (NRZ), RZ, VPPM, and PWM while concurrently providing dimming control. Operation is linear and flicker-free by implementing a negative feedback loop to control the maximum amount of current passing through the LEDs. Control blocks are integrated in a 1.5 × 1.5 mm^2 integrated circuit implemented in 180 nm CMOS process. This integrated system incorporates the feedback mechanisms to provide uniform light output together with the peak current control, which also prevents flickering. The proposed architecture is flexible enough to take any digital baseband modulation format. It provides linear 10–90 % dimming control while transmitting data.

The power consumption of on-chip circuitry, is negligible compared to the overall power consumption which yields an efficiency of 89 % at 120 mA of load

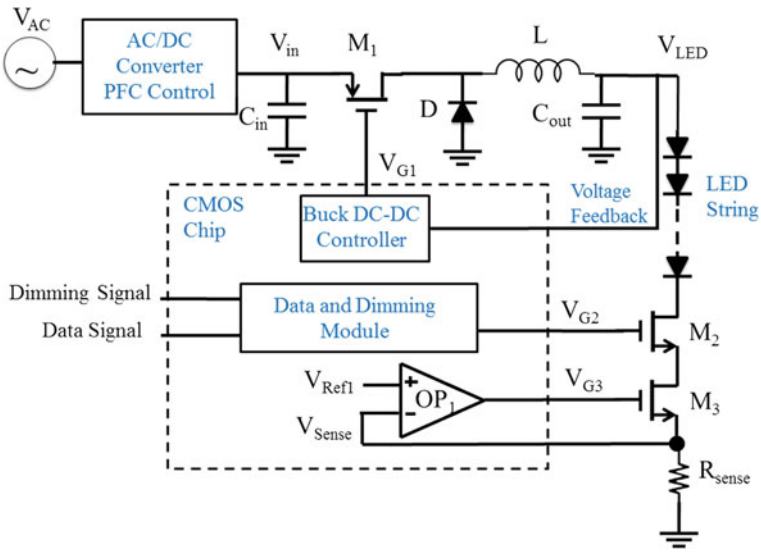

Fig. 18.5 Block diagram of LED driver utilizing digital modulation with dimming

current. The measured bit-error rate (BER) varies from 10^{-6} at the data rate of 2.5 Mbps to 10^{-3} at the data rate of 5 Mbps. All control functions integrated on-chip with the total power consumption of 5 mW and does not significantly degrade the overall driver efficiency. The design depicted in Fig. 18.5, is capable of taking any of digital data formats and applying the dimming control as well [3]. The commercial LED drivers have not yet been customized to be used for the VLC applications due to the low 3 dB bandwidth of switching power supply's control loop inherited in these drivers.

18.4.1 Buck Converter Design

The buck converter is a DC–DC converter used to step down the voltage and provides a regulated DC voltage. For the design of the LED driver, the buck converter is used for the DC–DC conversion mainly due to the fact that for most VLC applications the input power comes from the mains and in the case of low voltage high current LEDs, a high to low-power conversion is needed. Based on Fig. 18.5, this buck converter is composed of switches (MOSFET M_1 and Schottky diode D) and passive components (L and C_{out}). The steady state output voltage of the buck converter for a given duty ratio (D_r) of the PWM signal (V_{G1}), is calculated as $V_{\text{out}} = D_r \times V_{\text{in}}$. A feedback mechanism is needed to compensate for changes in D_r to guarantee a constant output voltage. To meet this goal, an on-chip buck controller circuit is implemented as shown in Fig. 18.5.

The transistor-level schematic of the buck controller circuit depicted in Fig. 18.6a includes voltage dividing resistors, R_{F1} and R_{F2}, to map the desired output DC voltage to the fixed reference voltage, V_{Ref2}. The negative feedback loop ensures that the output voltage is regulated based on the value of resistors R_{F1} and R_{F2}. The compensator circuit shapes the frequency response of the voltage feedback loop to maintain stability. The comparator block compares the output voltage of the error amplifier OP2, $V_{O,OP2}$, with a 300 kHz ramp signal, R_{amp1}, to produce the buck converter control signal, V_{G1}, which has a PWM waveform shape. As the buck converter output voltage, V_{LED}, swings above the reference voltage V_{Ref2}, the comparator output voltage falls, generating a PWM signal with smaller duty cycles. This duty cycle variation will affect the average time that the power MOSFET M_1 is turned on. This action forces the buck converter output voltage, V_{LED}, to drop until it reaches the desired value of 20 V. The circuit operates in a similar manner when the output voltage swings below the reference voltage. The buck converter is designed to provide 120 mA of current at the regulated output voltage of 20 V, with settling time of 120 μs. The open loop gain of the buck converter can be written as (18.1).

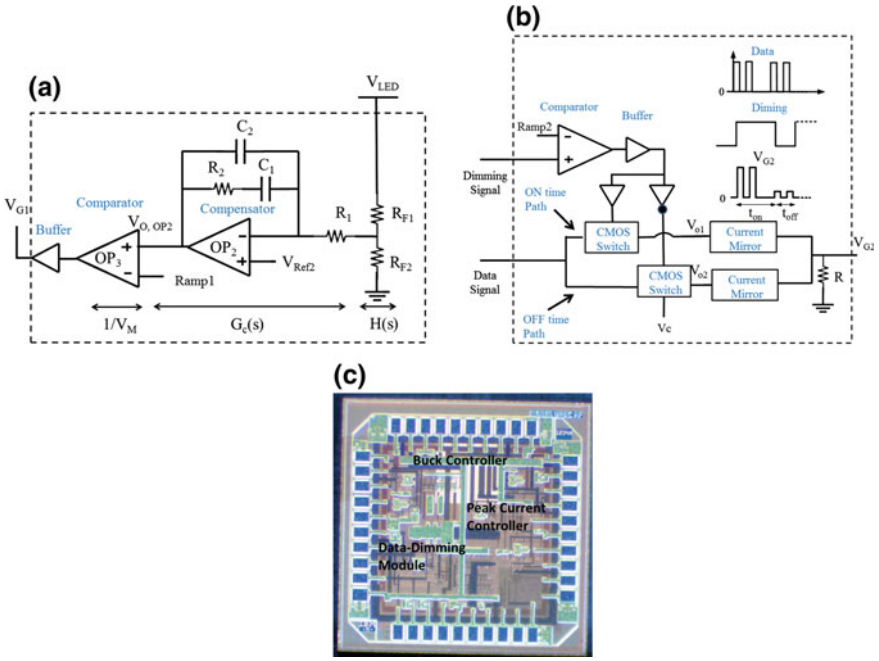

Fig. 18.6 180 nm chip block diagrams and its micrograph. **a** Buck DC–DC controller block diagram, **b** data and dimming block diagram, **c** chip micrograph

$$T(s) = G_c(s)(1/V_M)G_{vd}(s)H(s) \tag{18.1}$$

In (18.1), G_c is the transfer function of the compensator; $1/V_M$ is the gain of the pulse-width modulator; V_M is the peak value of the ramp signal applied to the input of comparator; G_{vd} is the transfer function of power section; and H is the sensor gain, as shown in Fig. 18.6a. The transfer function of the power section composed of L, C_{out} and the load is calculated as (18.2).

$$G_{vd}(s) = 1/\left(1 + s/(Qw_0) + (s/w_0)^2\right) \tag{18.2}$$

where $w_0 = 1/\sqrt{\text{LC}_{\text{out}}}$, $Q = R\sqrt{C_{\text{out}}/L}$, R is the equivalent load, and $H(s)$ is a fixed value proportional to the values of R_{F1} and R_{F2}. With the assumption of no compensating circuit, the open loop gain can be rewritten as (18.3).

$$T(s) = \alpha/\left(1 + s/(Qw_0) + (s/w_0)^2\right) \tag{18.3}$$

where α is a constant and is the multiplication of pulse-width modulator and sensor gain. Values of α, Q, and w_0 are selected in order to provide appropriate filtering and satisfy ripple requirements needed for the LED supply voltage, V_{LED}. It also forces the bandwidth of this transfer function, $T(s)$ in (18.3) to be limited in the kHz range due to the large values of L and C_{out}. The phase margin of this open loop transfer function is low based on the selected values of α, Q, and w_0 and is prone to instability [15]. To avoid reaching instability, a compensation method is required, such as dominant pole, integrator, lead, or lag compensation. The compensator based on integrator and lead method, shown in Fig. 18.6 is designed and its transfer function is given by (18.4).

$$G_c(s) = \frac{1 + s(R_2C_1)}{sR_1C_1(1 + C_2/\text{C}_1 + sR_2C_2)} \tag{18.4}$$

In this compensator, the zero is set to the resonant frequency to achieve a high phase margin. Also the pole corresponding to C_2 is set to diminish the gain of the $G_c(s)$ at high frequencies by choosing the ratio of $C_2 \cong C_1/10$. The LED driver circuit presented in this work overcomes the aforementioned bandwidth trade-off by utilizing the independent control of the DC–DC converter output voltage and the data-dimming signal to control LED current. The key design feature presented here involves isolating the data signal from this voltage feedback loop, and apply it independently. The circuit components highlighted in the dotted region of the proposed LED driver in Fig. 18.5 are implemented in a custom integrated circuit utilizing a 180 nm CMOS process. The peripheral components are designed to be off-chip and a power factor correction (PFC) unit might be added to suppress the total harmonic distortions as well.

18.4.2 Data-Dimming Multiplication Method

In the design shown in Fig. 18.5, the control of the LED power supply voltage is achieved by the buck converter circuit block while a separate data-dimming circuit module provides control signals for LED current waveform shaping for data transmission. This technique can be hired for applying to the off-the-shelf commercial LED drivers and make them suitable for operating in the VLC systems. The data-dimming module shown in Fig. 18.5 takes the dimming signal and generates its corresponding PWM signal. A digital multiplication method is employed to combine the PWM signal with the NRZ modulated data signal. The operational amplifier (Op-Amp) circuit OP_1, transistor M_3, and sensing resistor R_{sense} provide local feedback to maintain a constant average current through the LED for a given dimming level. This feedback also prevents flicker by controlling the amplitude of the LED's current. The amplitude is limited to a fixed value of V_{Ref1} divided by R_{sense}. The Op-Amp circuit is the most energy hungry element of the driver circuit. To improve driver efficiency, a novel on-chip compensation technique for the Op-Amp is implemented [16]. This compensator provides a high phase margin and extends the 3 dB bandwidth of the amplifier. This is achieved by generating the left-hand plane (LHP) zero using the passive RC network in the two stage trans-impedance amplifier. The combination of amplifier with its compensation design leads to a high gain-bandwidth, high slew rate design with the power consumption on the order of a few milliwatts ensuring the transmission of high data rate signals [16]. The data and dimming module as depicted in Fig. 18.6b, is responsible for combining the PWM and data signals. The dimming signal sets the brightness level of the light. The PWM dimming signal is generated by the comparison of dimming signal dc voltage with a 100 kHz ramp signal "R_{amp2}". The PWM dimming signal passes through the buffer and will be multiplied digitally with the incoming data signals utilizing CMOS switches. Here, as shown in Fig. 18.6b, two distinct sets of switches are employed, one of which operate over the 'on'-time and the other over the off-time. Due to the nature of the PWM signal, where its value is zero in the off-time, data will be lost during this time. To prevent this destructive accident from happening, an uninterrupted data transmission technique is chosen to allow data transmission during the PWM off-time; this is done by implementing a two-level drive current scheme such that the LEDs do not turn off completely in the off-time of PWM signal and some fraction of data will be injected in this period similar to the method explained previously in Fig. 18.3b; the amplitude of the signal in the off-time is smaller than the one in the on-time in order to provide the appropriate dimming levels. The ratio of this on-time signal to off-time signal is called R and the measurement results for different values of R are shown in the measurement results section. Selecting appropriate values for R is dependent on the dynamic range of the receiver and also the desired communication link range. Compared to the digital dimming approach of Fig. 18.3, the circuit

architecture presented here enables bi-level amplitude control, which is achieved with an external pin, V_c, as shown in Fig. 18.6b. This feature adds one degree of freedom to the circuit control by making the ratio of PWM on-time signal to off-time signal, R, under the user control. The output of the CMOS switches in both on and off-times will be converted to a current signal with the help of current mirrors and eventually this signal, V_{G2}, will be applied to the external MOSFET M_2 to drive the LEDs. The chip micrograph, shown in Fig. 18.6c, is composed of buck converter controller, data-dimming module, and peak current control. Using this method data can be detected at all the times in the receiver while the dimming capability is in place.

18.4.3 *Measurement Results of Digital Modulation with Dimming*

The LED driver should enable dimming control based on user settings, and also maintain communication link performance. The figure of merit for this driver circuit is based on dimming linearity during data transmission.

The data stream can take the form of any digital baseband modulation scheme, including NRZ, RZ, Manchester coding, and PPM signals. For the measurement purposes, a $2^7 - 1$ PRBS is generated and applied to the proposed LED driver. Dimming can be tuned based on the dimming signal input from 10 to 90 %. According to the measurement setup depicted in Fig. 18.7, the measurements are

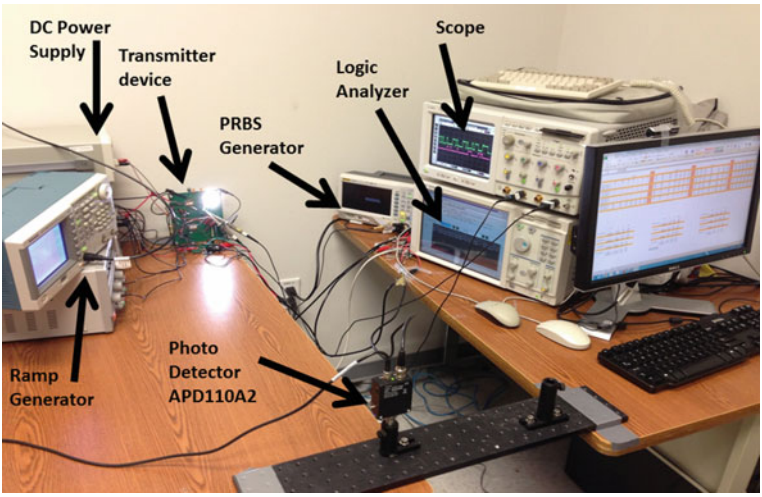

Fig. 18.7 Measurement setup developed for optical characterization of the LED driver circuit (the link range is 1 m)

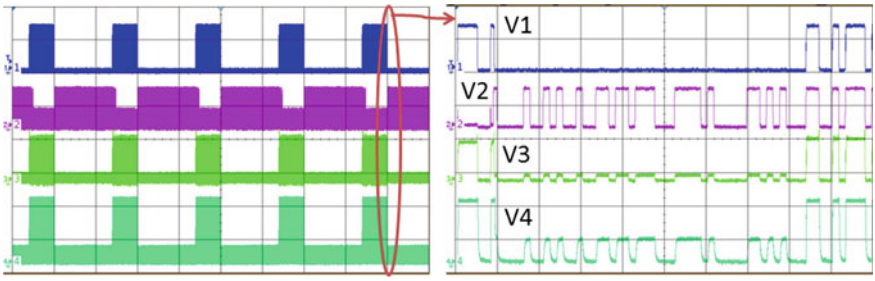

Fig. 18.8 Transient analysis of the LED driver chip and its zoomed-in view of transient signals with $2^7 - 1$ PRBS, NRZ modulated data signal and 30 % dimming level. *V*1: is V_{o1} in Fig. 18.6b, *V*2: is V_{o2} in Fig. 18.6b, *V*3: is Vsense in Fig. 18.5 which is proportional to LED current, and *V*4: is the received signal using the APD110A2 commercial receiver

performed at the link ranges of 30, 50, 70 cm, and 1 m. The VLC transmitter is biased using power supplies and the PRBS generator is connected to provide the appropriate generated data signal. A string of five LEDs (Cree MLCAWT) as the LED string in Fig. 18.5, the control signals, LED current, and the received signal, with the dimming ratio of 30 % and link range of 30 cm, are depicted in Fig. 18.8 together with its zoomed view of transient signals. The signal *V*1 and *V*2 are the V_{o1} and V_{o2} in Fig. 18.6b, respectively.

As it is shown in this figure, some portion of data is included in the off-time of the PWM waveform. For this measurement, a commercial Thorlabs APD110A2 photo-receiver is used. The Agilent 16702B logic analysis system is used for calculating the BER of the system. The transmitted data sequence and the received signal at the output of the APD110A2 photo-receiver are both connected to the logic analyzer. The Sync output from the PRBS generator is also connected to the logic analyzer to provide a Clock signal. For measuring the BER, the digitized transmitted data and received signal are compared off-line for different values of data rates and different values of link ranges. The measured BER versus the data rate is depicted in Fig. 18.9 for link ranges of 30, 50, 70 cm, and 1 m. For the link range of 30 cm, the BER varies from 10^{-6} at the data rate of 2.5 Mbps to 10^{-3} at 5 Mbps. Figure 18.10 shows how the BER varies with the change in dimming ratio.

In Fig. 18.10, R is the ratio of on-time to off-time of PWM signal. To have an uninterrupted detection of data, some portion of data is placed inside the off-time of PWM signal to make it practical to detect data at all the times. There is a trade-off between BER, link range, and brightness control based on the selection of R. In this design, the value of 20 % provides acceptable brightness control from 10–90 %. Figure 18.11 shows the eye diagram at data rates of 5 and 10 Mbps both for link ranges of 50 cm and 1 m. While maintaining the data transmission, a LED driver should provide the uniform output light and a linear change of light based on the dimming levels.

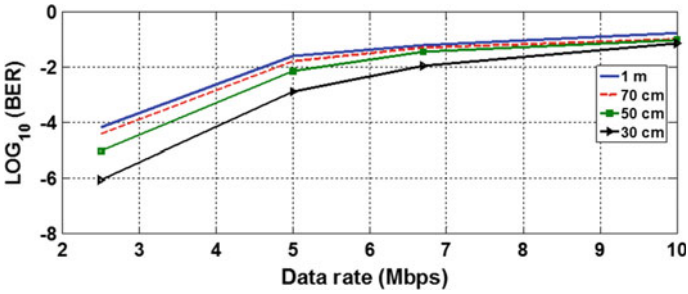

Fig. 18.9 BER versus data rate for different link ranges

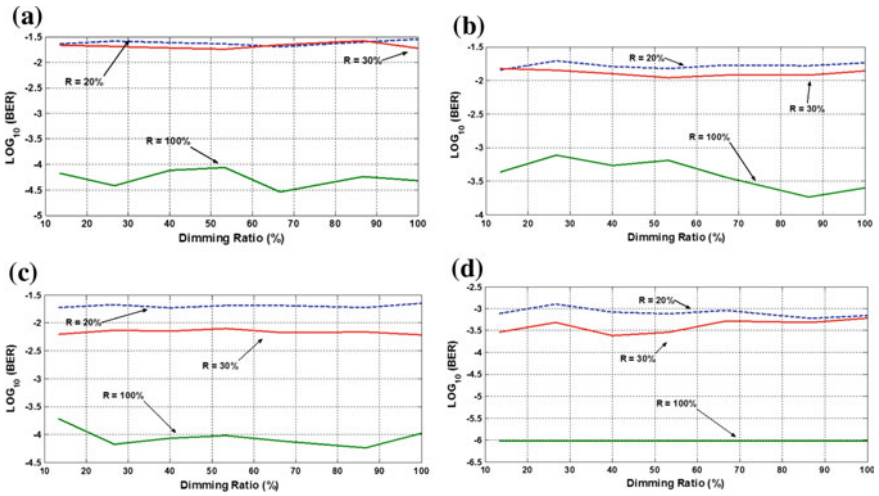

Fig. 18.10 Variation of BER versus dimming ratio for 5 Mbps data rate (*R* ratio of on-time to off-time of PWM signal), **a** Link range of 100 cm, **b** Link range of 70 cm, **c** Link range of 50 cm, **d** Link range of 30 cm

Figure 18.12 shows the linear change of brightness level based on the dimming ratio and link range. Figure 18.12a shows the change of illuminance (Lux) versus the data rate. Figure 18.12b shows the change of Lux versus the dimming ratio. As it is depicted in this figure, the brightness varies linearly from 10–90 % for data rates of 2.5, 5, 7, and 10 Mbps. Table 18.1 summarizes the characteristics of the proposed LED driver. For efficiency calculation, the losses due to the following components are considered: Schottky diode (D), equivalent series resistance (ESR) of capacitor and inductor, MOSFETs, M_1, M_2, and M_3, (switching and conduction losses), series resistance of LEDs and sensing resistor (R_{sense}). Component values considered for the efficiency calculation are listed in Table 18.1.

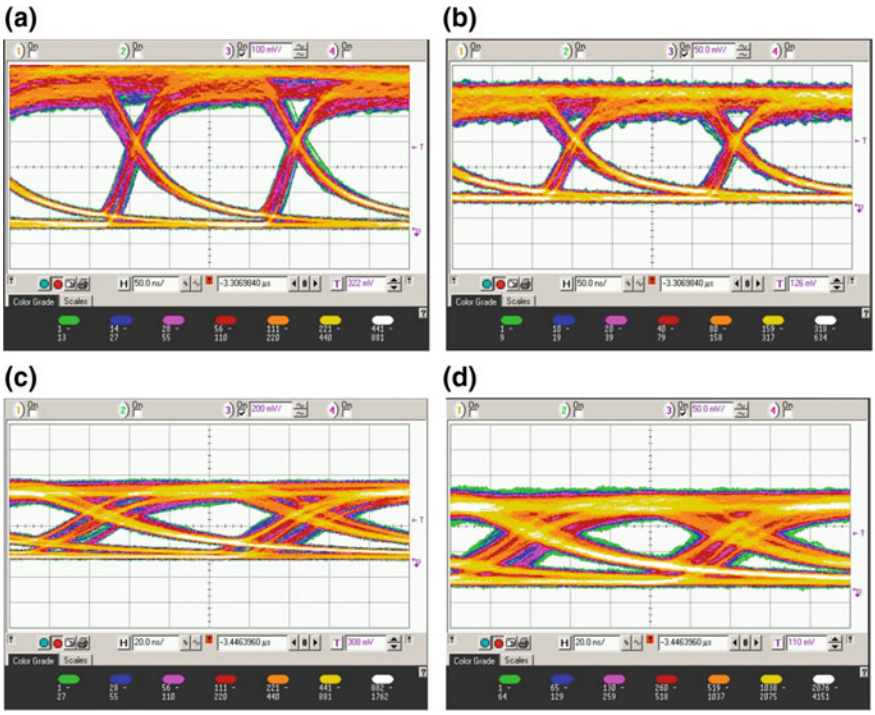

Fig. 18.11 Eye diagrams: **a** Data rate of 5 Mbps, link range of 50 cm, **b** Data rate of 5 Mbps, link range of 1 m, **c** Data rate of 10 Mbps, link range of 50 cm, and **d** Data rate of 10 Mbps, link range of 1 m

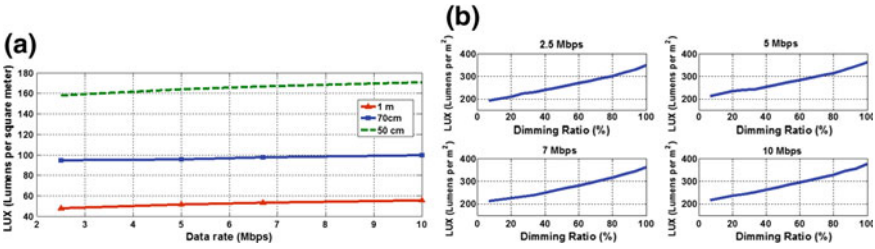

Fig. 18.12 Lux measurements: **a** Lux versus data rate. **b** Lux versus the dimming ratio for different data rates at link range of 30 cm

The efficiency is calculated as output power to the summation of output power and the total losses. The chip power consumption is also taken into account regardless of its negligible effect. Based on this calculation, the efficiency of the proposed LED driver is 89 % at an LED drive current of 120 mA.

Table 18.1 Chip and buck converter performance

Chip performance					
Process	Area (mm^2)	On-chip consumption power (mW)	Dimming ratio	Efficiency	Supply voltage (V)
180 nm CMOS	1.5 × 1.5	5	10–90 %	89 % at 120 mA	1.8
Buck converter performance					
LED	LED current (mA)	Settling time (μs)	Output ripple/V_{LED}	Switching frequency (kHz)	V_{in}/V_{LED} (V)
Xlamp ML-C	120	120	0.002	300	25 V/20 V
R_1 (MΩ)	R_2(kΩ)	C_1(pF)	C_2(pF)	R_{F1}(MΩ)	R_{F1}(kΩ)
1.2	128	100	10	2.12	100
M_1	M_2, M_3	R_{sense} (Ω)	L(μH)	D	C_{out} (μF)
IRLMS5703PbF	2N7002	5	33	MSS1P5	5

18.5 Analog Techniques

In addition to single-carrier pulsed modulation techniques including NRZ-OOK, RZ-OOK, and PPM, multi-subcarrier modulation (MSM) techniques for VLC are also proposed [17]. OFDM is a practical realization of data transmission using MSM, where high data rates can be achieved through parallel transmission of high-order multilevel quadrature amplitude modulation (M-QAM) symbols on orthogonal subcarriers. The analog OFDM signal offers distinct advantages over pulsed schemes. For example, the spectral efficiency of OFDM is attractive to overcome the limited modulation bandwidth of LED optical sources, thus constitutes a hot research topic in the field of VLC.

In general, the output of a conventional RF-based OFDM modulator is complex. In intensity modulation with direct detection (IM/DD) systems, quadrature modulation is not possible and a real-valued OFDM signal is required. Therefore, the OFDM commonly used in RF communications must be modified [18]. As shown in Fig. 18.13, two conventional schemes are used to realize a real-valued OFDM signal suitable for IM/DD, namely, DC biased optical OFDM (DCO-OFDM) and asymmetrically clipped optical OFDM (ACO-OFDM). A real OFDM signal can be generated by constraining the input to the inverse fast Fourier transform (IFFT) operation to have Hermitian symmetry. According to Fig. 18.13, the serial data bits are grouped into symbols and modulated using a QAM modulator. The mapper assigns the QAM symbols to the IFFT operation input bins (OFDM subcarriers). The OFDM time-domain symbols are available after the IFFT operation. Different OFDM schemes for VLC (real-valued OFDM symbol) are realized based on how the QAM symbols are assigned to the subcarriers (Mapping). The bipolar DCO-OFDM symbol is used to modulate the optical carrier intensity after setting a

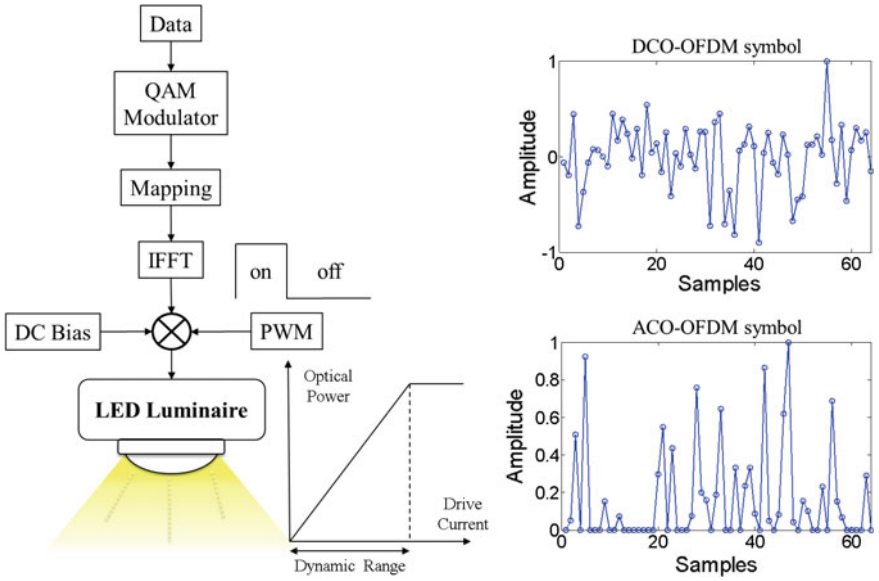

Fig. 18.13 Building blocks of a VLC OFDM modulator with dimming and LED dynamic range constraint

proper DC operating point. In ACO-OFDM, the generated bipolar symbol is converted to unipolar through clipping of all negative values at zero.

VLC research to date has primarily been focused on achieving increasingly high data rates. Assuming near-field communication in a static scenario, recent experimental setups have been demonstrated to achieve Gbps VLC links [19]. According to the laboratory conditions of these demonstrations, the human factors component and illumination features for a realistic illumination and communication system have been largely overlooked. Such research is vital to the adoption of VLC. Thus, additional research focus is necessary to examine its effect on light functionality and quality in practical scenarios [20]. As a modulation suitable for dimming, OFDM is not acceptable by itself, but can be combined with other dimming techniques. If such schemes coupled with intensity and color control techniques prove to be acceptable to the human eye, OFDM stands to be a forefront contender in the future of practically adoptable VLC systems that satisfy lighting requirements.

Research efforts are conducted to assist in developing approaches to address the challenge of incorporating OFDM with high-quality illumination and lighting state control. In [21], the performance of the ACO-OFDM is investigated under different brightness conditions. The dimming functionality is realized based on the analog dimming approach, where the ACO-OFDM signal superimposed on a DC bias point. Here, the effective brightness or the dimming set point is determined by the DC current associated to the bias point as well as the average current that corresponds to the ACO-OFDM signal. The nonlinear behavior of the LED is included in the simulation model [22].

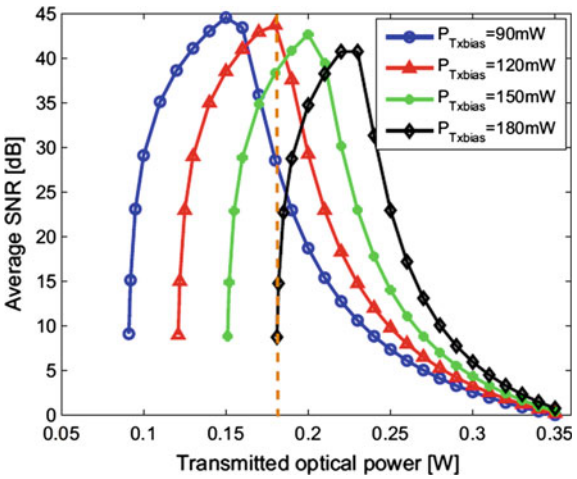

Fig. 18.14 Average SNR versus the transmitted optical power utilizing analog dimming

For different DC biasing optical power, the obtained signal-to-noise ratio (SNR) values versus the transmitted optical power are shown in Fig. 18.14. The SNR improves, as expected, with the increase of the useful optical signal power reaching an optimal value for a specific DC biasing optical power. By further increasing the useful optical signal power, the SNR starts to deteriorate as a result of induced nonlinear distortions caused by the LED limited dynamic range. Signal clipping is more pronounced in this case and the clipping noise becomes significant, i.e., additive white Gaussian noise (AWGN) noise dominates at low SNR values and clipping distortion dominates at large SNR values.

An important observation is that by properly setting the biasing power, an optimum SNR is obtained for a wide range of brightness levels. Accordingly, the ACO-OFDM signal amplitude should be adaptively scaled to control the effective brightness and to minimize the induced noise due to signal clipping. Such signal power dependence of induced nonlinear effects clearly limits the maximum achievable data rates. The DC bias point should also be changed adaptively to maximize the useful dimming range and to maintain a good SNR.

An OFDM signal can also be cast onto the PWM dimming-controlled signal (see Fig. 18.13). In [23], the time-domain OFDM symbols are transmitted onto the PWM signal only during the "on-state". However, this limits data throughput to the relatively low PWM line rate of commercial LED drivers that is around tens of kHz. In [24], the LED drive current is the time-domain OFDM signal multiplied by a periodic PWM pulse train. Achieving high-speed links with this approach is only feasible when the PWM dimming signal is at least twice the frequency assigned to the largest subcarrier frequency of the OFDM signal to avoid subcarrier interference. However, this constraint is not practical for commercial LEDs with limited modulation bandwidth and limits the opportunity to use COTS LED drivers.

Therefore, dimming compatible OFDM schemes must consider existing LED and driver technologies. For instance, the proposed reverse polarity optical OFDM

(RPO-OFDM) approach utilizes the entire period of a PWM signal for OFDM signal transmission, maintaining the data rate for a wide dimming range independent of the PWM frequency [25]. This approach also maintains the signal within the dynamic range constraint of the LED. In RPO-OFDM, both OFDM and PWM signals contribute to the effective brightness. The basic idea is superimposing the OFDM signal on top of the PWM dimming signal. For example, and assuming an ACO-OFDM signal and a known dimming set point, conventional ACO-OFDM symbols are superimposed during the off-time of the PWM signal and flipped (reverse polarity) ACO-OFDM symbols are added during the on-time of the PWM signal. It is also worth pointing out that RPO-OFDM can also be applied to any bipolar or unipolar OFDM format.

As shown in Fig. 18.15, the PWM signal current $i_{\mathrm{PWM}}(t)$ pulsating between I_L and I_H is shown. I_H is assumed to correspond to the maximum allowed LED current $i_{\mathrm{LED}}(t)$ and I_L corresponds to the minimum $i_{\mathrm{LED}}(t)$ according to the LED data sheet, i.e., the LED dynamic range can be denoted by I_H-I_L. In the proposed system, the OFDM signal current $i_{\mathrm{OFDM}}(t)$ is superimposed on $i_{\mathrm{PWM}}(t)$ after setting a proper polarity of the individual ACO-OFDM symbols using a RPO-OFDM modulator depending on whether the symbol is being transmitted on I_H or I_L during the PWM signal period T_{PWM}. To explain the idea of RPO-OFDM with an example, the duty cycle D = 20 %, 10 ACO-OFDM symbols, OFDM time-domain samples i_k = 64 and $T_{\mathrm{PWM}} = 10 \times T_{\mathrm{OFDM}}$ are assumed, where T_{OFDM} is the OFDM symbol period. Consequently, the polarity of the first two ACO-OFDM symbols is reversed, i.e., −ve polarity, then transmitted on the I_H followed by 8 ACO-OFDM symbols, i.e., +ve polarity, transmitted on I_L. At the receiver side, and after time-synchronization, all 640 samples are extracted and the polarity of the first 128 samples is readjusted. Figure 18.16 shows ACO-OFDM symbols that are sequentially transmitted at

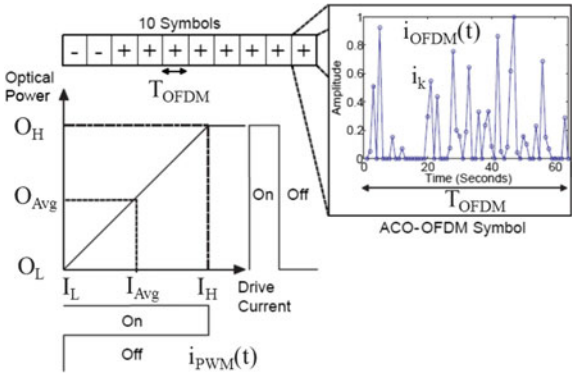

Fig. 18.15 An example to demonstrate the proposed RPO-OFDM system: based on the dimming level, i.e., D, the polarity of the OFDM symbols are adjusted before the OFDM signal is superimposed on the PWM signal. The nonlinear transfer function of the LED: O_L denotes the output optical power corresponding to the input current I_L and O_H denotes the output optical power corresponding to the input current I_H

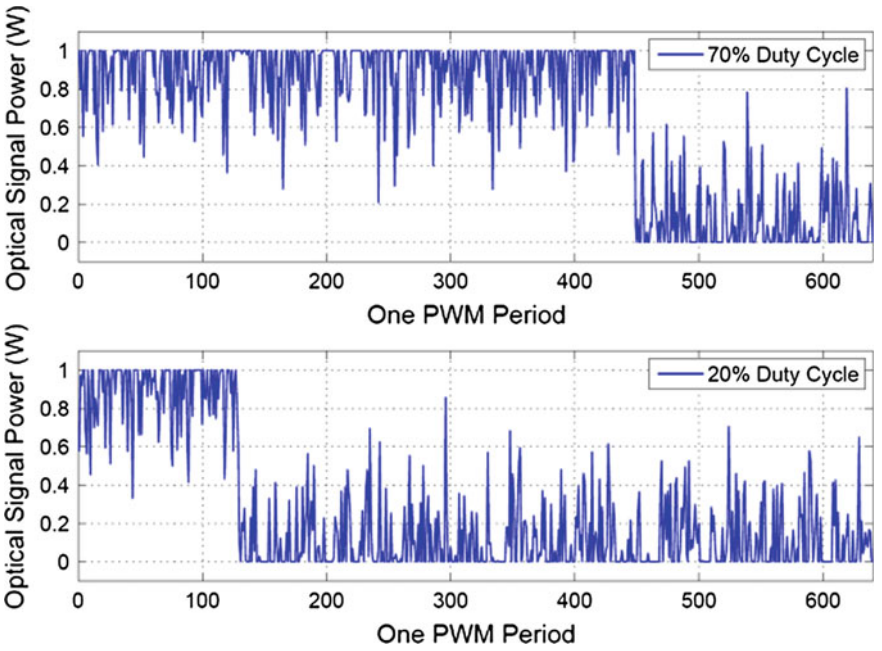

Fig. 18.16 RPO-OFDM signal waveform based on ACO-OFDM at 70 % (*upper*) and 20 % (*lower*) duty cycles

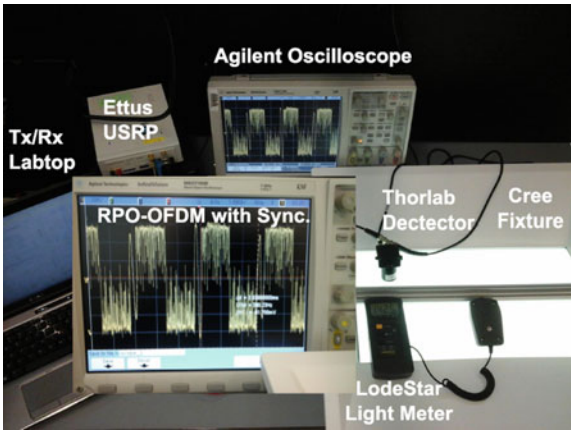

Fig. 18.17 Proof-of-concept testbed showing D = 50 % RPO-OFDM signal based on ACO-OFDM [26]

D = 20 % and D = 70 %. In [26, 27], testbeds are used to demonstrate VLC transmission using RPO-OFDM to achieve dimming compatibility with the industry-standard PWM signal (see Fig. 18.17). A linear control of the brightness is confirmed while maintaining the target data rate.

18.6 Conclusions and Future Directions

With LEDs being increasingly used in different illumination applications, the necessity for an efficient driver with an optimized control circuitry becomes more important. It is a necessity to ensure LED driver compatibility with data modulation schemes for use in VLC based applications. Conventional LED drivers incorporate circuitry to provide a constant supply voltage and current regulation of LED devices. The design trade-offs between feedback loop bandwidth, switching losses, and ripple rejection impose limitations on data modulation rates of VLC transmitters using commercial LED driver architectures. The LED driver's architecture also depends on the type of modulation scheme adopted. For the baseband modulation techniques such as OOK, implementing dimming control is straightforward. However, this is not the case for analog modulation schemes. Even though the RPO-OFDM is one solution for this problem, more research is required in this area. The trend in LED driver design in lighting is towards efficiency, but speed for modulation is also required if VLC is sought. Hence, energy and speed trade-offs must be made to meet overall goals. Accordingly, the design trend is toward integration and the target is a product that is fast, low cost, and low power.

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