**For error correction :**

$$\text{If } i \neq j \text{ , } ( e_i \neq e_j )$$

$$w_i = v_1 \oplus e_i \qquad v_1, v_2 \in U \text{ ( fault - free )}$$
$$w_j = v_2 \oplus e_j$$

$$\text{Then} \qquad s_i = Hw_i \neq s_j = Hw_j$$

$$s_i = Hw_i = H ( v_1 \oplus e_i ) = Hv_1 \oplus He_i = 0 \oplus He_i = He_i$$
$$s_j = Hw_j = He_j$$

$$\text{Since } e_i = 0 \ldots 0 \underset{i}{1} 0 \ldots 0$$

$$He_i = h_i \text{ - } i^{th} \text{ column in H} \quad \Rightarrow \quad h_i \neq h_j$$
$$He_j = h_j \text{ - } j^{th} \text{ column in H} \qquad\quad h_i \neq 0$$

<u>Conclusion :</u> **To correct all single errors matrix H should contain *different nonzero columns.***

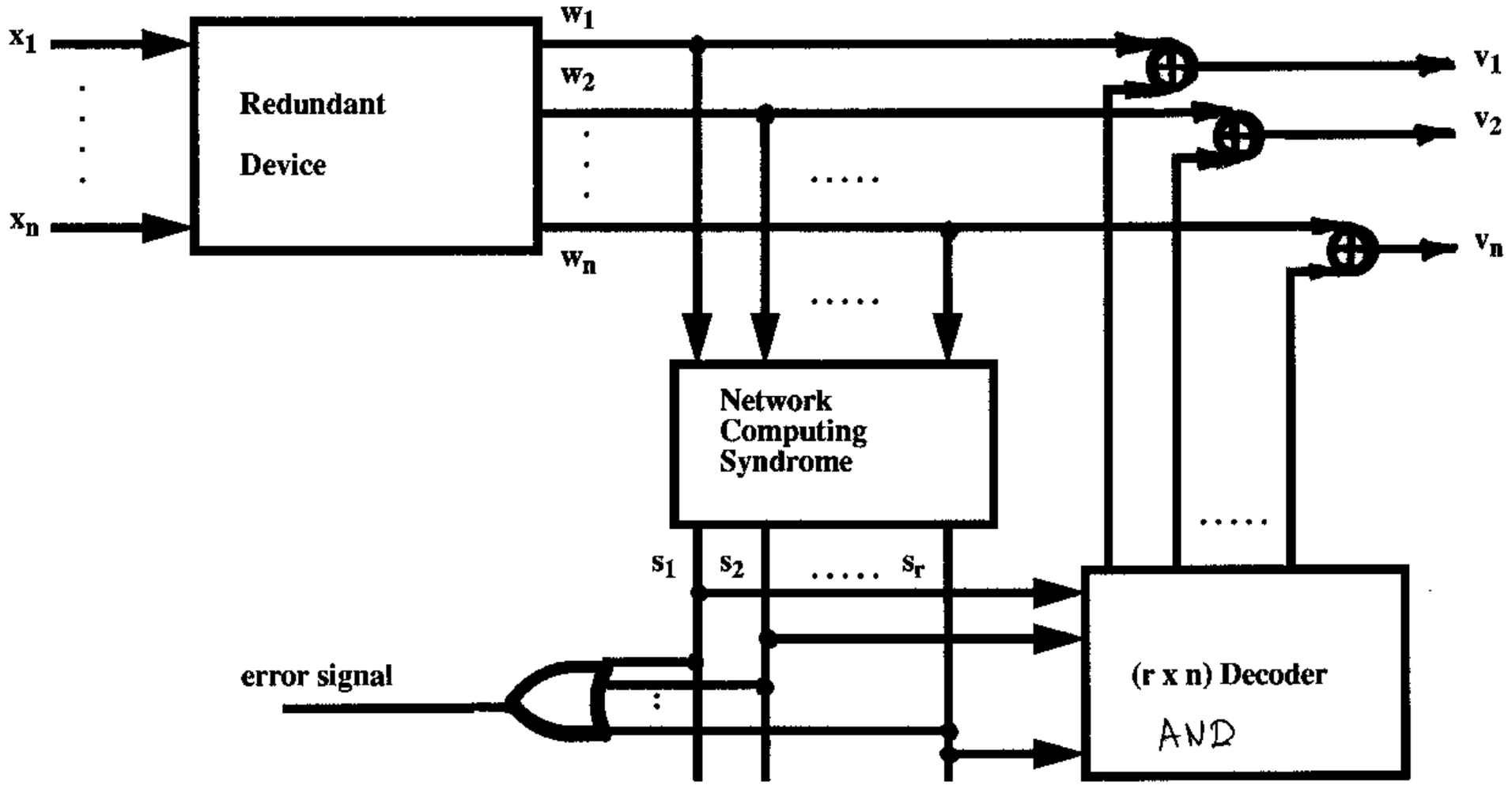
$$r = \lceil \log_2 ( n + 1 ) \rceil$$

## Error Detection / Correction by Hamming Codes.

$r = \lceil \log_2 (n+1) \rceil$, $\quad n = k + r$

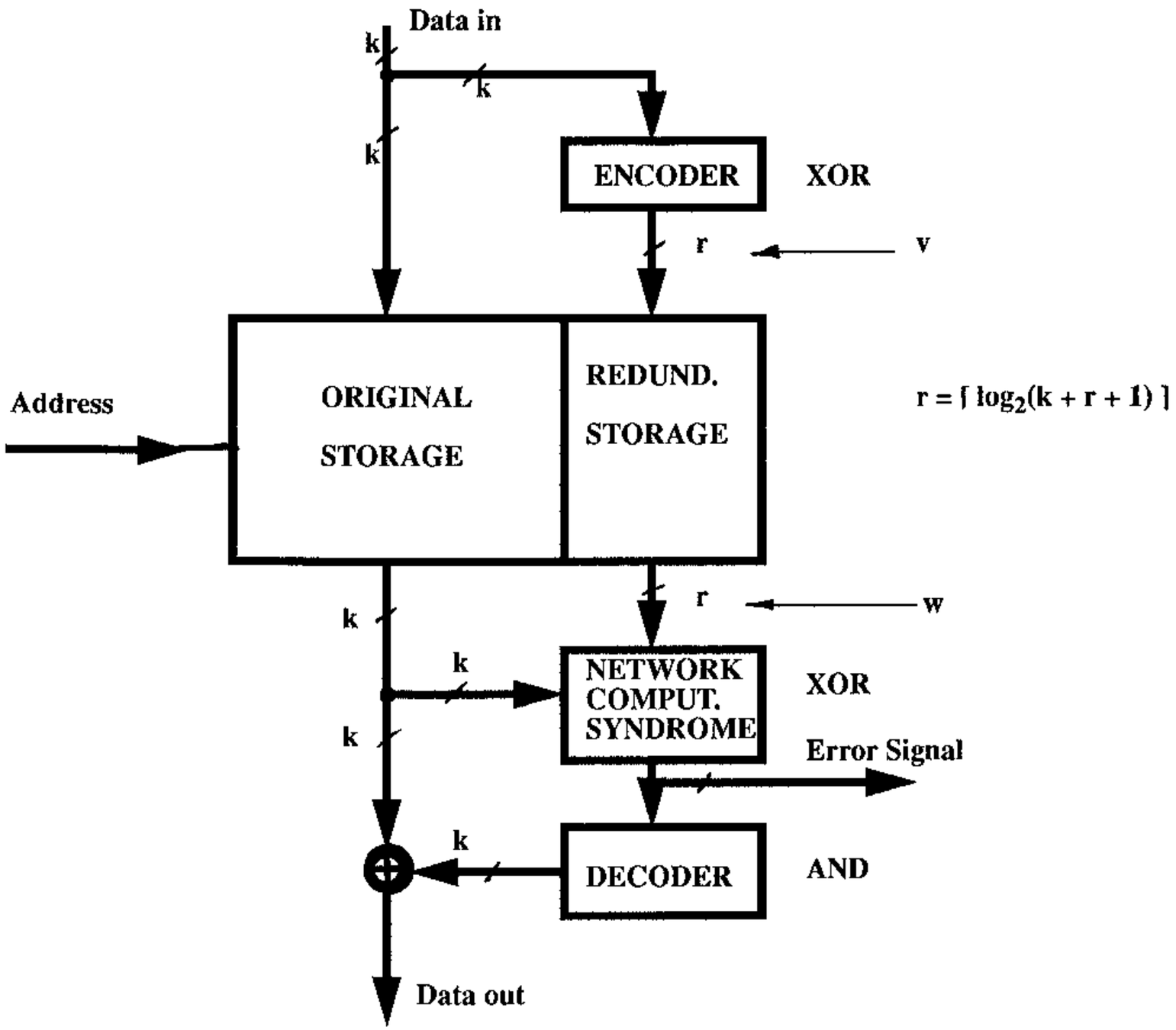
$(v_1, \ldots, v_n)$ - correct output

$(w_1, \ldots, w_n)$ - distorted output



## Correction of Single Errors in RAM by Hamming Codes.

**(one bit in *every cell* may be distorted)**




$$r = \lceil \log_2(k + r + 1) \rceil$$

**Syndrome :** $s = (s_1, s_2, s_3)$

$$H = \begin{bmatrix} 1 & 2 & 3 & 4 & 5 & 6 & 7 \\ 0 & 1 & 1 & 1 & 1 & 0 & 0 \\ 1 & 0 & 1 & 1 & 0 & 1 & 0 \\ 1 & 1 & 0 & 1 & 0 & 0 & 1 \end{bmatrix}$$

$s = (0, 0, 0) \Rightarrow$ no errors

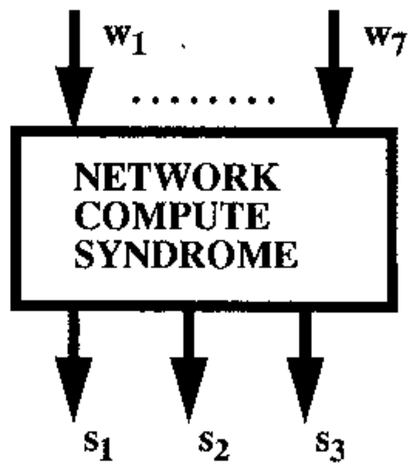
If s is equal ith column H $\Rightarrow$ error in the bit i.

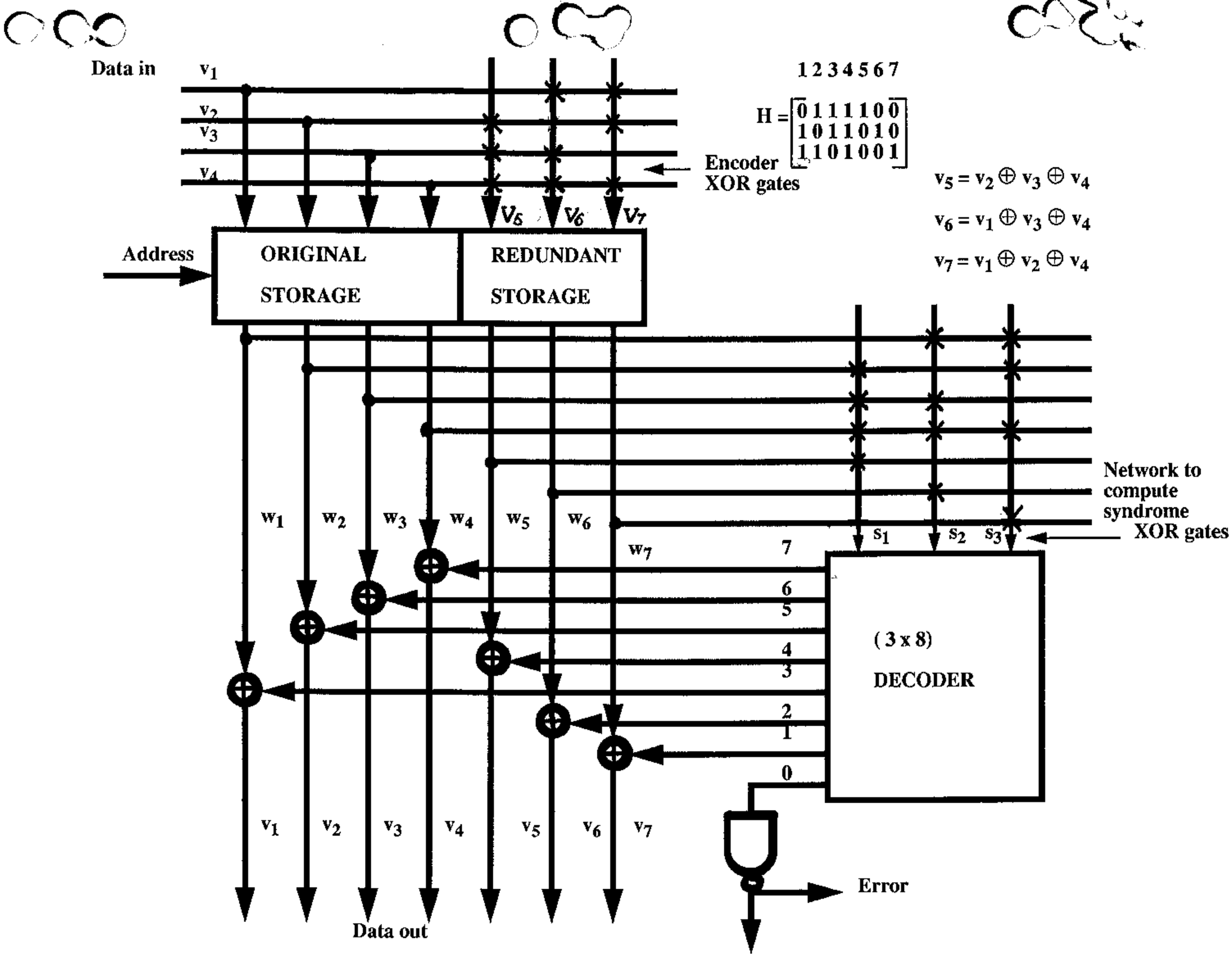
$$s_1 = w_2 \oplus w_3 \oplus w_4 \oplus w_5$$

$$s_2 = w_1 \oplus w_3 \oplus w_4 \oplus w_6$$

$$s_3 = w_1 \oplus w_2 \oplus w_4 \oplus w_7$$

Example : If $s = (1\ 0\ 1) \Rightarrow$ error in the bit 2




Data in
$v_1$
$v_2$
$v_3$
$v_4$
$v_5$
$v_6$
$v_7$
1 2 3 4 5 6 7
H = 0 1 1 1 1 0 0
1 0 1 1 0 1 0
1 1 0 1 0 0 1
Encoder
XOR gates
$v_5 = v_2 \oplus v_3 \oplus v_4$
$v_6 = v_1 \oplus v_3 \oplus v_4$
$v_7 = v_1 \oplus v_2 \oplus v_4$
Address
ORIGINAL STORAGE
REDUNDANT STORAGE
Network to compute syndrome
XOR gates
$w_1$ $w_2$ $w_3$ $w_4$ $w_5$ $w_6$ $w_7$
$s_1$ $s_2$ $s_3$
7
6
5
4
3
2
1
0
( 3 x 8)
DECODER
Error
$v_1$ $v_2$ $v_3$ $v_4$ $v_5$ $v_6$ $v_7$
Data out

## EXAMPLE $K=4$, CORRECT $\ell=1 \Rightarrow$

$$r \geq \lceil \log_2(K+r+1) \rceil \Rightarrow r=3$$

$$H = \begin{pmatrix} 0 & 0 & 1 & 0 & 1 & 1 & 1 \\ 0 & 1 & 0 & 0 & 1 & 1 & 0 \\ 1 & 0 & 0 & 1 & 1 & 0 & 1 \end{pmatrix}$$ CHECK MATRIX

$$v \in V \Leftrightarrow Hv = 0$$

## EQUATIONS FOR ENCODER

$$\left.\begin{aligned} v_3 &= v_5 \oplus v_6 \oplus v_7 \\ v_2 &= v_4 \oplus v_6 \oplus v_7 \\ v_1 &= v_4 \oplus v_5 \oplus v_7 \end{aligned}\right\}$$

$v_4, v_5, v_6, v_7$ are <u>INFO</u> BITS

$v_1, v_2, v_3$ are <u>check</u> BITS

## EXAMPLE (CONT'D)

# EQUATIONS FOR SYNDROME COMPUTATION

$$\left.\begin{aligned} S_1 &= W_3 \oplus W_5 \oplus W_6 \oplus W_7 \\ S_2 &= W_2 \oplus W_4 \oplus W_6 \oplus W_7 \\ S_3 &= W_1 \oplus W_4 \oplus W_5 \oplus W_7 \end{aligned}\right)$$

$$(v_1, v_2, v_3, v_4, v_5, v_6, v_7) \xrightarrow{\text{error}}$$

$$\rightarrow (w_1, w_2, w_3, w_4, w_5, w_6, w_7)$$

# EXAMPLE (CONT'D)