Detection of Single Errors.

Parity Checking.

d(U) = 2

One equation (r = 1) : $(v_1, \ldots, v_n) \in U$ if $v_1 \oplus v_2 \oplus \ldots \oplus v_n = 0$

k = n - 1

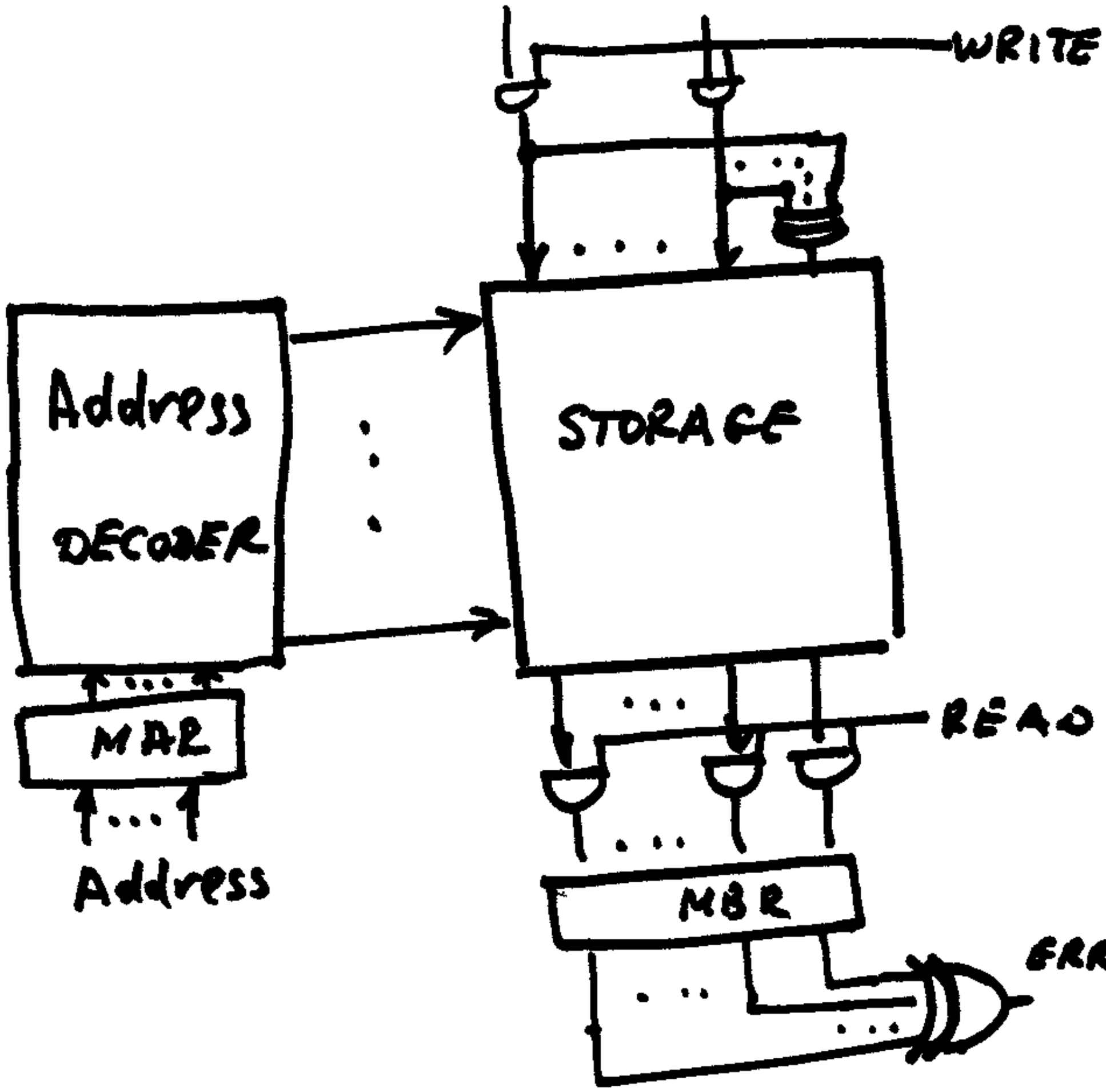
Detects all errors of *odd* multiplicities used for memories and busses.

Example : **n = 4 , k = 3**

v_1	v_2	v_3	v_4	
0	0	0	0	← parity (check) bit
0	0	1	1	
0	1	0	1	
0	1	1	0	
1	0	0	1	
1	0	1	0	
1	1	0	0	
1	1	1	1	

Lecture 9 ESE 353

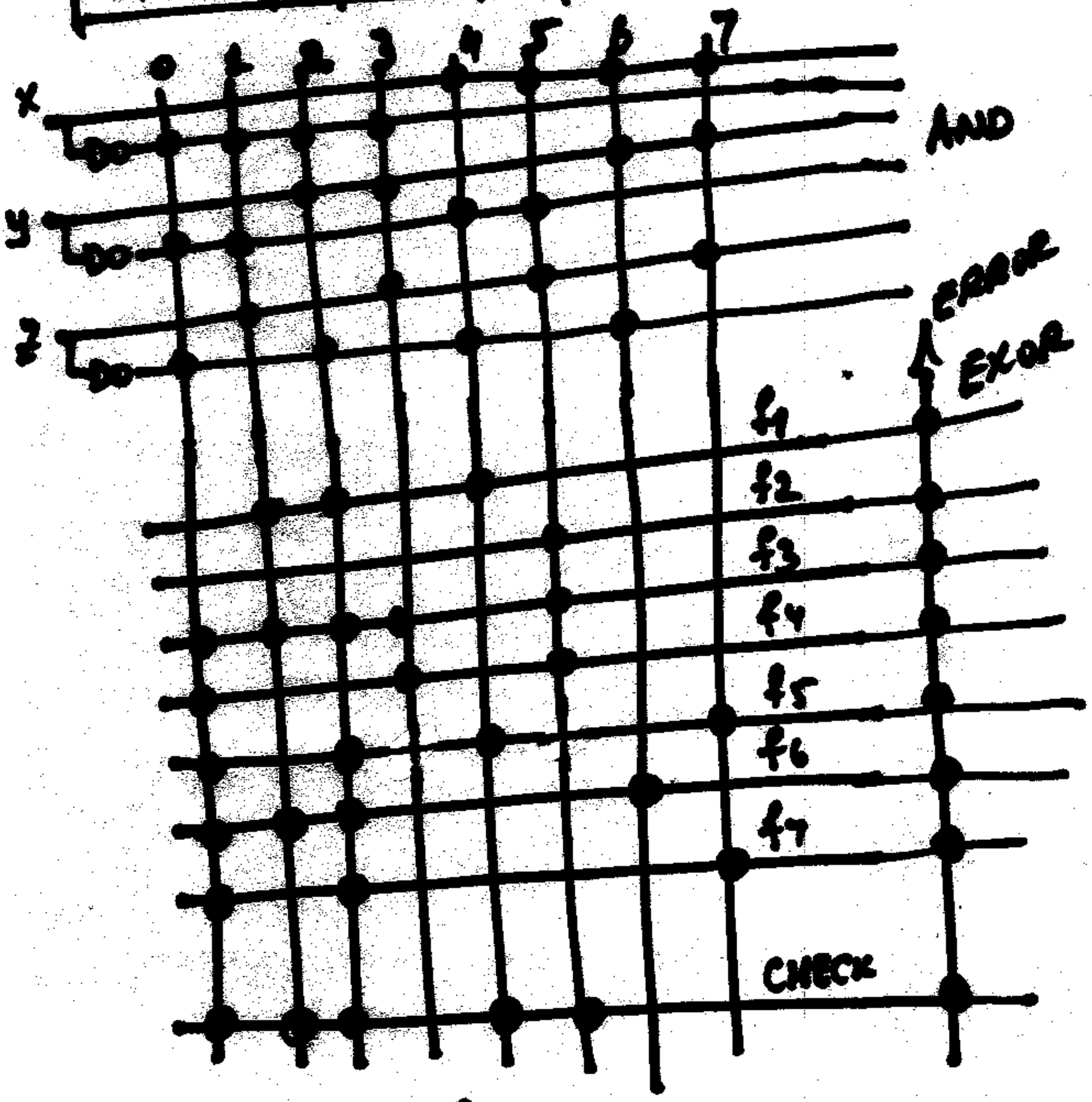
MEMORY WITH PARITY CHECKING



PARITY PREDICTION FOR PLAS

2166

EXAMPLE	m=3			k=7		r=2		
NUMBER	f_0	f_1	f_2	f_3	f_4	f_5	f_6	CHECK
0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1	1
2	0	0	0	0	1	1	0	1
3	0	0	0	1	0	1	1	0
4	0	0	1	0	0	1	1	0
5	0	1	0	0	1	0	1	1
6	0	1	0	1	0	0	0	1
7	0	1	1	0	0	0	0	1



OR

Self - Error Detection Based on Parity Prediction.

Example : *Binary Adder.*

$s = a + b$

$a = (a_{k-1}, \ldots, a_0, a_c)$

$b = (b_{k-1}, \ldots, b_0, b_c)$

$s = (s_{k-1}, \ldots, s_0, s_c)$

a_c , b_c , s_c - check bits.

$$a_c = \bigoplus_{i=0}^{k-1} a_i$$

$$b_c = \bigoplus_{i=0}^{k-1} b_i$$

$$s_c = \bigoplus_{i=0}^{k-1} s_i$$

Let c_i (i = 1, . . . , k-1) is the carry from (i - 1)th bit.

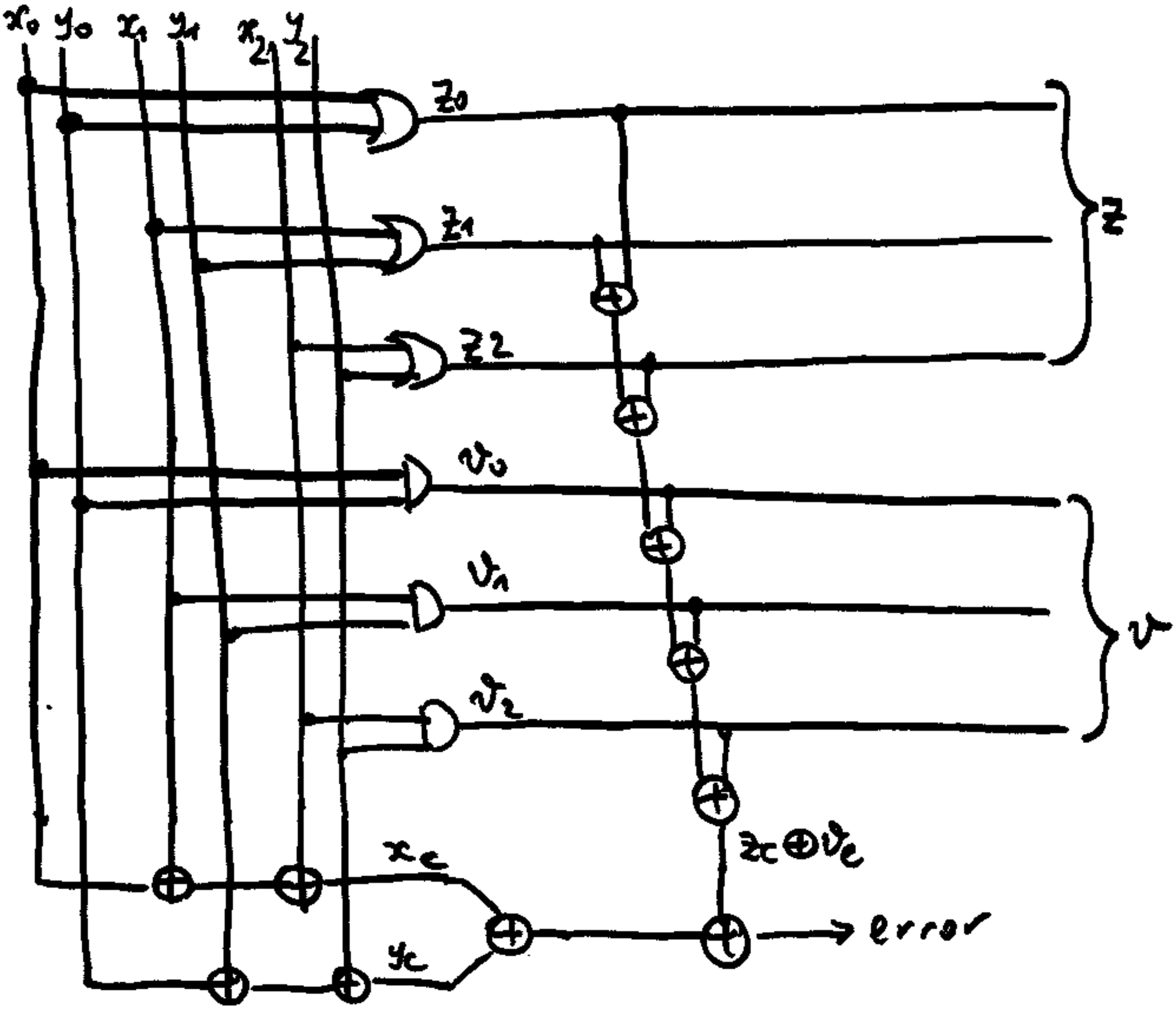
Then

$$s_c = \bigoplus_{i=0}^{k-1} s_i = \bigoplus_{i=0}^{k-1} a_i \oplus \bigoplus_{i=0}^{k-1} b_i \oplus \bigoplus_{i=0}^{k-1} c_i = a_c \oplus b_c \oplus \bigoplus_{i=0}^{k-1} c_i$$

In the next fig. carry circuits are *duplicated* to avoid propogation of errors.

D. K. Pradhan " Fault Tolerant Computing"
vol 1, ch 5, Prentice Hall.

EXAMPLE $m=3$



Any single error in $(\underbrace{z_0, z_1, z_2, v_0, v_1, v_2}_{\text{output}})$ is detected

Any single error in $(\underbrace{x_0 y_0, x_1, y_1, x_2 y_2}_{\text{INPUT}})$ is detected

Since x_i is involved in computing three parity bits z_c, v_c and x_c

(y_i is involved in z_c, v_c, any y_c)