Gate-Level Fault Masking

Interwoven Logic

COMBINATION OF VOTING AND COMPUTING

Critical faults ⇒ force a certain gate output

Subcritical faults ⇒ do not force a gate output

Gate	Critical Faults	Subcritical Faults
AND	1 → 0	0 → 1
OR	0 → 1	1 → 0
NOT	0 → 1, 1 → 0	None
NAND	1 → 0	0 → 1
NOR	0 → 1	1 → 0
XOR	None	0 → 1, 1 → 0

(9)

Interwoven Logic: critical faults at one layer result in output errors which are subcritical input faults for the following layer-

Any fault is stopped within two layers

All - NAND networks or alternating layers of AND and OR gates

Very high redundancy

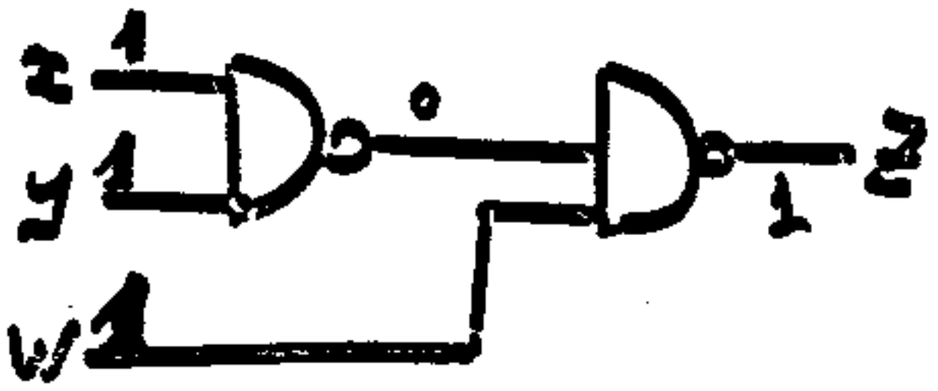
INTERWOVE LOGIC: NAND NETWORKS

EVERY BIT X replaced by (x_1, x_2, x_3, x_4)

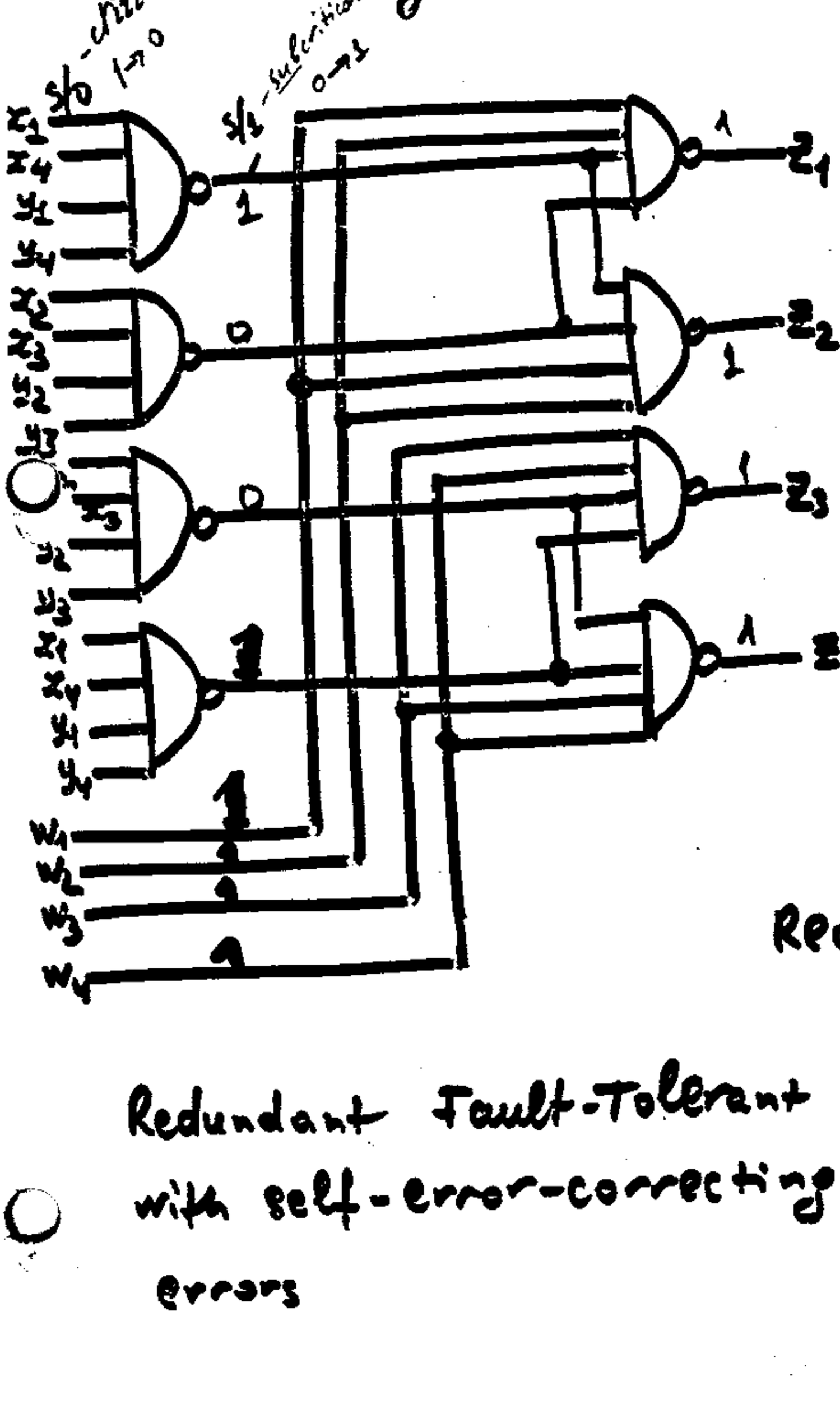
EVEN LAYERS: GROUPING: $\{x_1, x_4\}, \{x_2, x_3\}$

ODD LAYERS GROUPING: $\{x_1, x_2\}, \{x_3, x_4\}$

Example



Original Non redundant device



$x \Rightarrow (x_1, x_2, x_3, x_4)$

$y \Rightarrow (y_1, y_2, y_3, y_4)$

$z \Rightarrow (z_1, z_2, z_3, z_4)$

$w \Rightarrow (w_1, w_2, w_3, w_4)$

quadded logic

Redundancy R = 2.

Redundant Fault-Tolerant device with self-error-correcting of single errors

Interwoven Logic

To correct t errors:

1. Redundancy $R = (t+1)^2$ in a number of gates ($t=1 \Rightarrow R=4$)
2. Every gate has $(t+1)$ times more inputs than the corresponding gate in the original device

Very expensive!

(D. P. Sawiorek, R. S. Swarts, "The Theory and Practice of Reliable System Design: Digital Press, 1982, C4.3)