SC 753: SCANDAL (13)

On-Line Self-Testing of Gate Arrays (PLAs)

Unidirectional faults (BERGER CODES)

Error:

$0 \longmapsto 1$

		Redundancy
fault-free:	1 1 $\overset{*}{0}$ 1 0 0 1 0 1 1 $\overset{*}{0}$ 1 1 0	0 1 1 $\overset{*}{0}$
faulty:	1 1 1 1 0 0 1 0 1 1 1 1 1 1 0	0 1 1 1

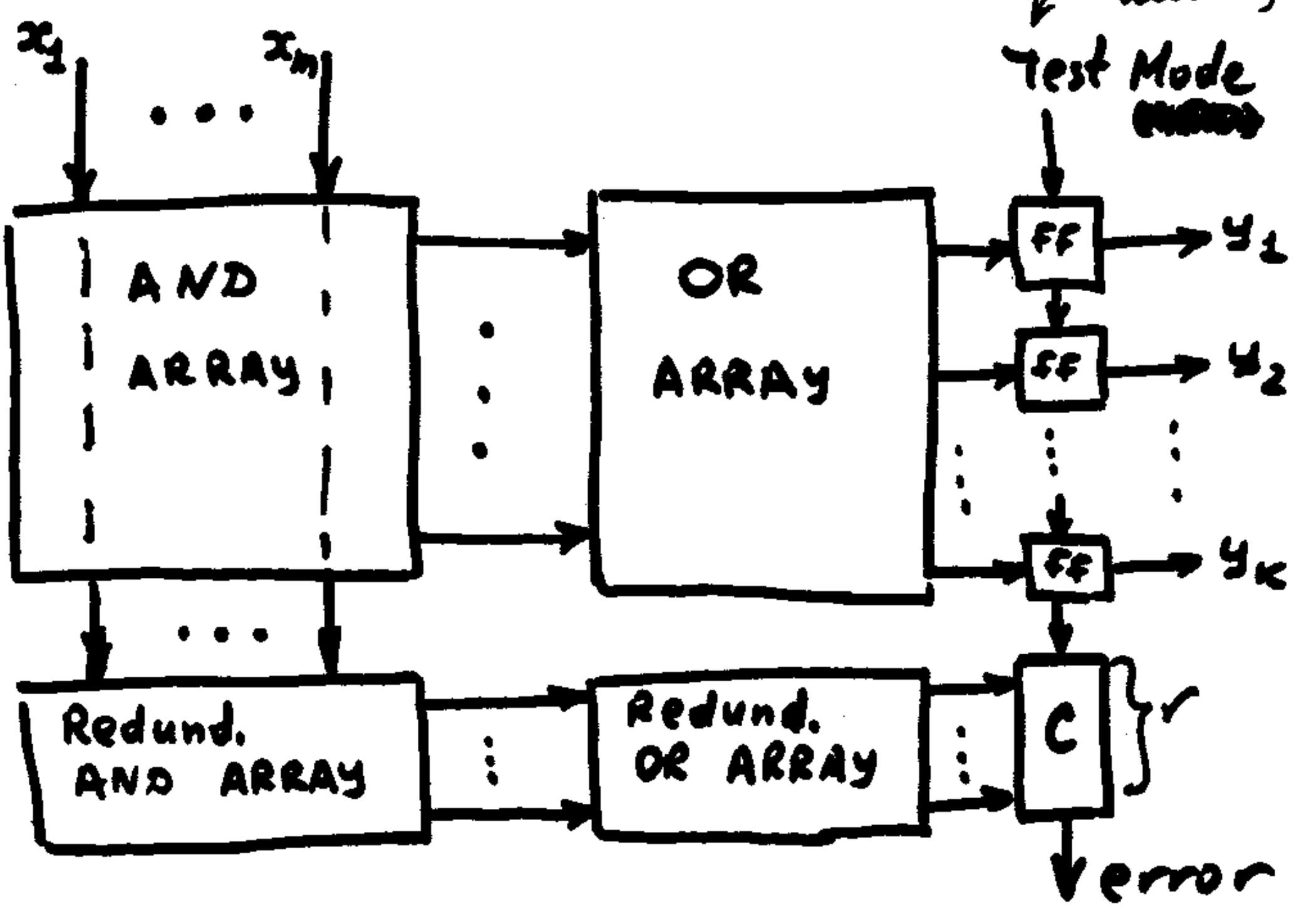
In the redund. part ⇒ the binary representation of a number of 0's in information bits

All unidirectional faults with any multiplicity are detected

Self-Testing PLAs (STPLA)

Most faults (>95%) are unidirectional

Block-diagram STPLA

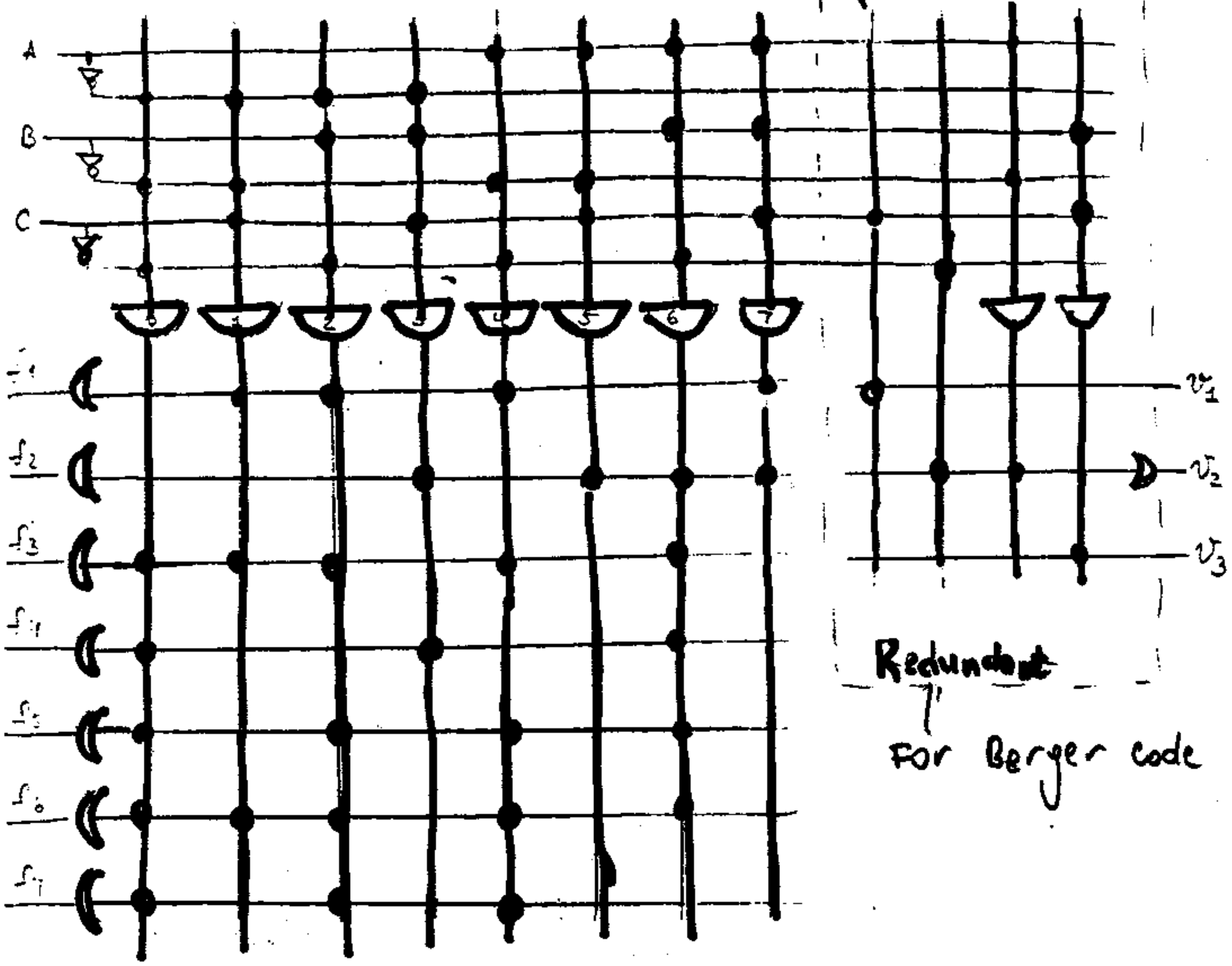


C - counter (r Bits) (COUNT DOWN)

Redundancy about (10-15)%

Example $m = 3, k = 7 \Rightarrow r = 3$

A	B	C	f_1	f_2	f_3	f_4	f_5	f_6	f_7	Berger code: Redundant bits v_1	v_2	v_3	Modified Berger code: Redund. bits v_1	v_2
0	0	0	0	0	1	1	1	1	1	0	1	0	0	0
0	0	1	1	0	1	0	0	1	0	1	0	0	0	1
0	1	0	1	0	1	0	1	1	1	0	1	0	0	0
0	1	1	0	1	0	1	0	0	0	1	0	1	1	0
1	0	0	1	0	1	0	1	1	1	0	1	0	0	0
1	0	1	0	1	0	0	0	0	0	1	1	0	1	1
1	1	0	0	1	1	1	1	1	0	0	1	0	0	0
1	1	1	1	1	0	0	0	0	0	1	0	1	1	0



All SSFs are detected (except for input stuck-at faults)

Redundancy estimations

K - number of outputs in a PLA

N_0 - max number of 0s in an output vector (fault-free)

r - number of redund. outputs (number of FFs in the counter)

$$r \le \lceil \log_2(N_0+1) \rceil \le \lceil \log_2(K+1) \rceil.$$

Modified Berger codes

Let $n_1, n_2, \dots, n_t$ are different numbers of 0s in output vectors for the original device $0 \le n_1 < n_2 < \dots < n_{t-1} \le N_0$

For the previous example $n_1 = 2$, $n_2 = 4$, $n_3 = 5$, $n_4 = 6$

Encode $n_1 \leftrightarrow \overbrace{00\dots00}$ - redundand bits

$n_2 \leftrightarrow 00\dots01$

$n_3 \leftrightarrow 00\dots10$

$$r = \lceil \log_2 t \rceil$$

See example at the previous page

where $2 \leftrightarrow 00$, $4 \leftrightarrow 01$, $5 \leftrightarrow 10$, $6 \leftrightarrow 11$

$r = 2$

Example!

(24, 48, 28) PLA $\Rightarrow$ $r = 5 = \lceil \log_2 29 \rceil$

Every product term contains 8 literals;
every output is OR of at most 24 product terms

Number of equivalent NAND gates

original PLA : 1130

redund. PLA : 1235

about 10% gate redundancy

Error detecting capability of Berger codes

1. All SSFs at lines with equal parity are detected (unidirectional errors)

2. All errors of odd multiplicity in info bits are detected

3. All SSFs in the output register and output counter are detected

4. For even multiplicity $\ell = 2s$ errors in info bits we have for prob. of masking

$$P = \binom{2s}{s} / (2^{+2s} - 1) \text{ very small}$$

K out of m codes

These codes are nonlinear, nonsystem. (cannot distinguish between information and check bits)

K out of m codes are nonsystematic and for $k=\lceil m/2 \rceil$ are optimal (have more code-words than Berger codes of the same length)

Example $m=4$, $k=2$

Code:

0011
0101
1001
0110
1010
1100

Number of code words (fault-free outputs) is:

$$\binom{m}{k}$$

In most cases $k \simeq m/2$

for large m $\binom{m}{m/2} \simeq \frac{2^m}{\sqrt{2\pi m}}$

$\pi = 3.14$

Error Detecting Capability of K out of m codes

dist = 2

detects: all errors of odd multiplicity.
about 50% of double errors
for large m

All unidirectional faults (like Berger codes, but K out of m is not systematic)

Disadvantages

∴ large amount of redundancy ⇒
∴ circuitry for parallel detection of errors is complex
∴ for serial detection this circuitry is simple (one counter)

K out of m codes have been used in control circuitry

Example BELL ESS-3a 4 out of 8 code for microstore

DETECTION OF UNIDIRECTIONAL FAULTS BY BERGER CODES AND K OUT OF M CODES

EXAMPLE $V = a + b$ $a = (a_0, a_1)$

2-bit adder $b = (b_0, b_1)$

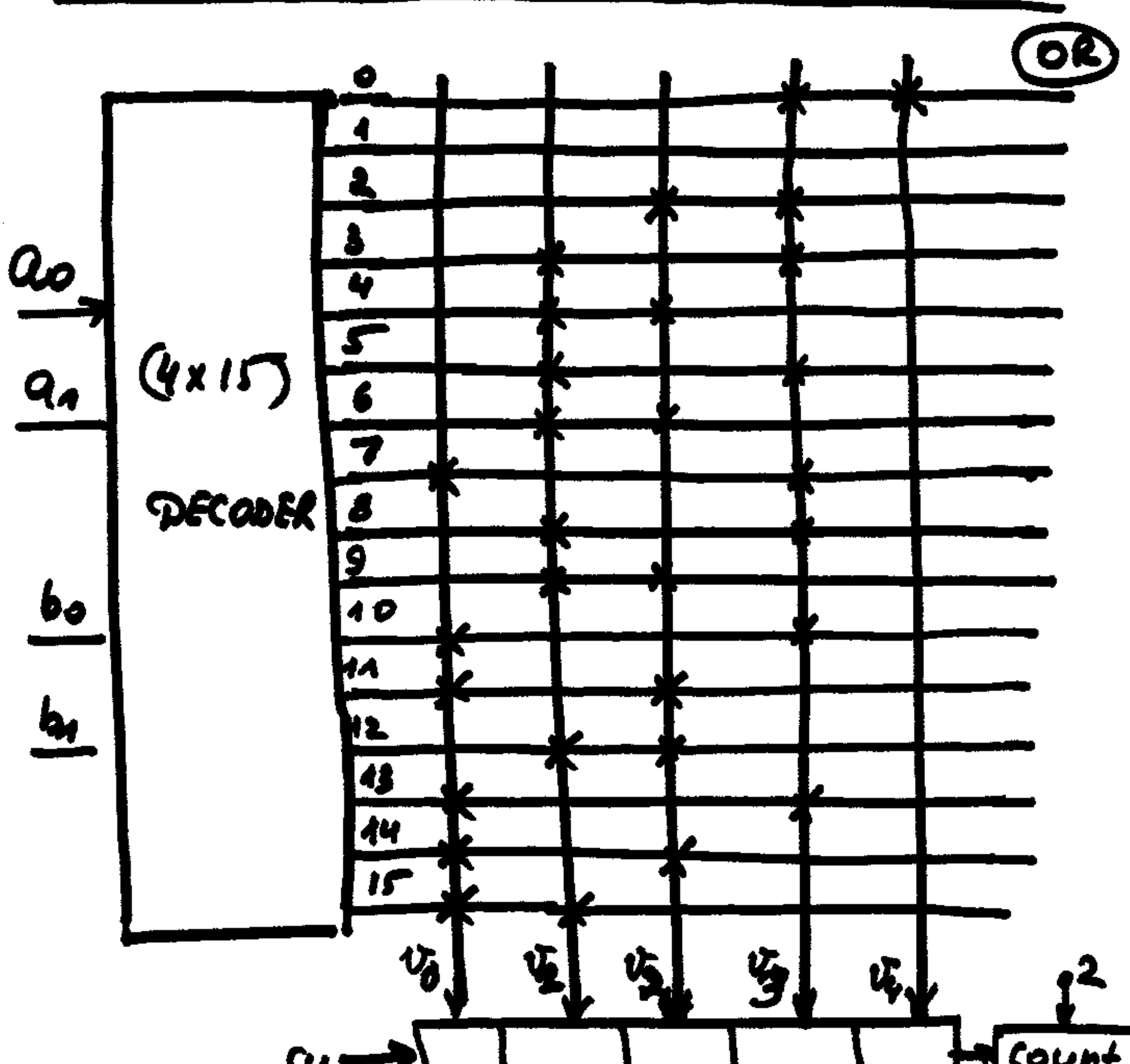
$V = (v_0, v_1, v_2)$

a_0	a_1	b_0	b_1	v_0	v_1	v_2	v_3	v_4	v_3	v_4
0	0	0	0	0	0	0	1	1	1	1
0	0	0	1	0	0	1	1	0	1	0
0	0	1	0	0	1	0	1	0	1	0
0	0	1	1	0	1	1	0	1	0	0
0	1	0	0	0	0	1	1	0	1	0
0	1	0	1	0	1	0	1	0	1	0
0	1	1	0	0	1	1	0	1	0	0
0	1	1	1	1	0	0	1	0	1	0
1	0	0	0	0	1	0	1	0	1	0
1	0	0	1	0	1	1	0	1	0	0
1	0	1	0	1	0	0	1	0	1	0
1	0	1	1	1	0	1	0	1	0	0
1	1	0	0	0	1	1	0	1	0	0
1	1	0	1	1	0	0	1	0	1	0
1	1	1	0	1	0	1	0	1	0	0
1	1	1	1	1	1	0	0	1	0	0

FOR BERGER CODE

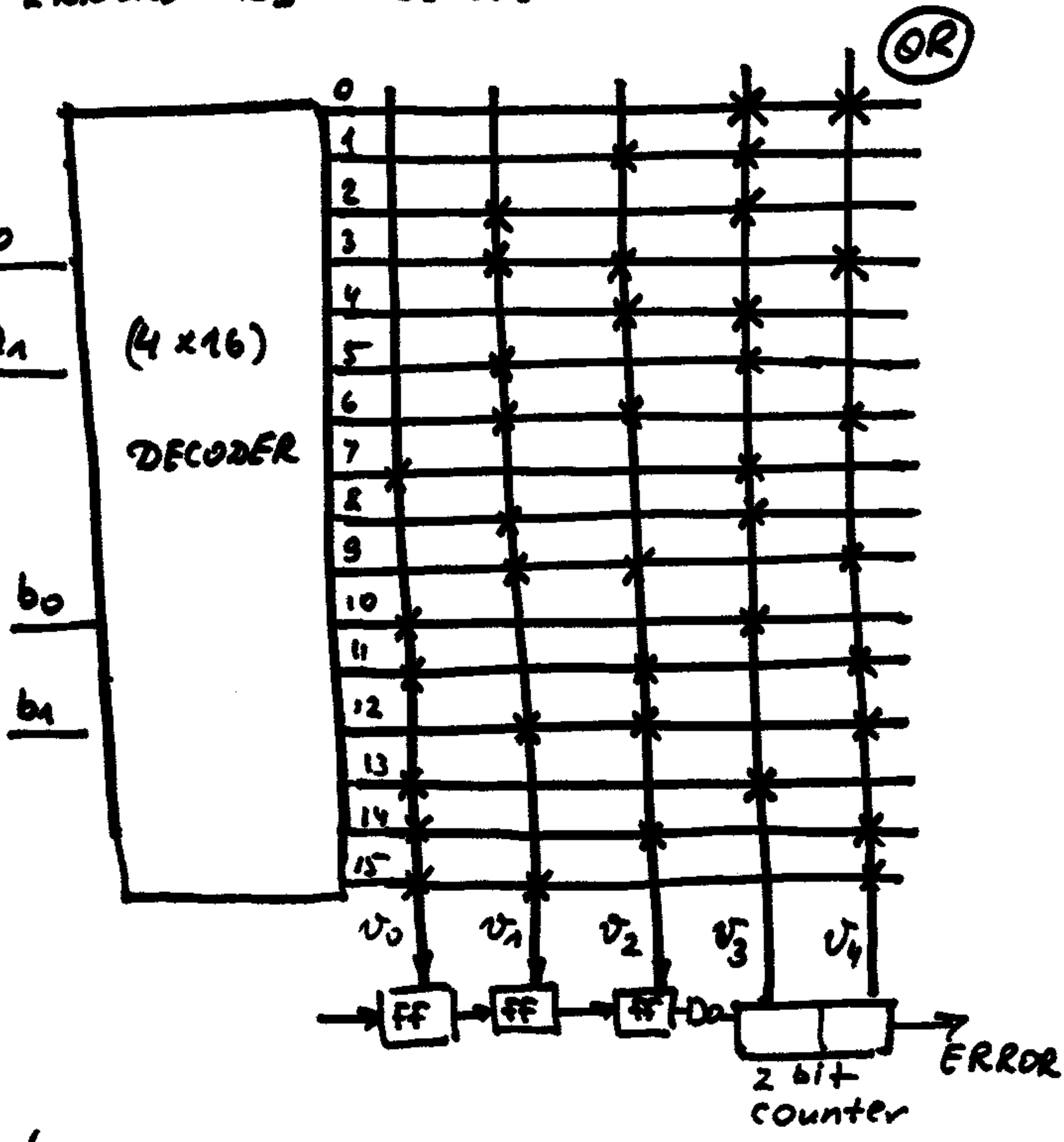
FOR 2 out of 5 CODE

IMPLEMENTATION OF 2-bit ADDERS WITH DETECTION OF UNIDIRECTIONAL ERRORS BY 2 Out of 5 CODES



For any a_0, a_1, b_0, b_1
there are exactly two ones in
$(v_0, v_1, v_2, v_3, v_4)$

IMPLEMENTATION OF 2-bit Adder WITH DETECTION OF UNIDIRECTIONAL ERRORS BY BERGER CODES



(v_3, v_4) represent number of 0s in (v_0, v_1, v_2)