SC 753

FAULT-TOLERANT COMPUTING

LECTURE NOTES

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Complimentary Text:

"FAULT-TOLERANT COMPUTING"
Edited by D.K. PRADHAN

Related courses:

SC561 ERROR CONTROL CODES

SC752 TESTING OF COMPUTER HARDWARE

SC891 RESEARCH SEMINAR.

Fault Models

Fault (failure) is a physical event

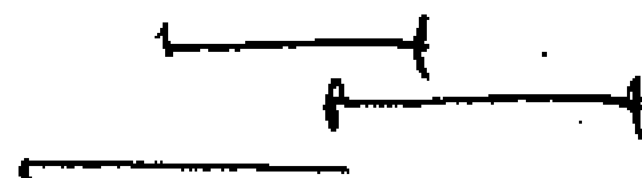
Error is a manifestation of a fault

Logic-level faults VS TIME FAULTS

Fault model is necessary for efficient test generation AND TEST OBSERVATION AND DFT

Statistical analysis of faults to construct fault models.

Fault model depends on implementations and environments.



Standard Fault Models

I. Stuck-at faults - a line Z is stuck-at-0 or stuck-at-1 (Z/0 , Z/1 or Z≡0, Z≡1)

Single (SSF) and multiple (MSF) faults

SSF is the most popular model

Stuck-at faults are detected by off-line and by on-line testing

Fault coverage - percentage of faults which are detected)

(Example: For SSF and μprocessors 95% is a reasonable fault coverage)

Number of stuck-at faults with a multiplicity at most l

$$\sum_{i=1}^{l} 2^i \binom{L}{i} ; \quad \binom{L}{i} = \frac{L!}{i!(L-i)!} ; \quad a! = 1\cdot 2\cdot 3\cdot \ldots \cdot a$$

L is a number of lines in a network

SYMMETRICAL FAULTS

Example $L = 1{,}000$, $l = 2$

$2 \cdot 10^6$ faults

INDEPENDENT ERRORS

Prob of a FAULT WITH MULTIPLICITY l at given l lines is p^l

Special Classes of Stuck-at Faults

∴ Bursts of length b (for discs or tapes)

FOR SOLID BURSTS

Number of Bursts: $N-b+1$ N is a number of binary cells

∴ Symmetric, asymmetric and unidirectional stuck-at faults

Number of unidirectional faults with a multiplicity at most l: $\sum_{i=1}^{l} \binom{L}{i}$ Ex: $L=1{,}000$; $l=2 \Rightarrow 500{,}500$ faults

∴ Input / Output (Terminal or Pin) stuck-at faults at interconnections between chips

Number of I/O Stuck-at faults for a chip with m inputs and K outputs: $\sum_{i=1}^{l} 2^i \binom{m+K}{i}$; Ex: $m=K=16$; $l=2 \Rightarrow 2{,}048$ faults (symmetrical)

Fault Models (Cont.)

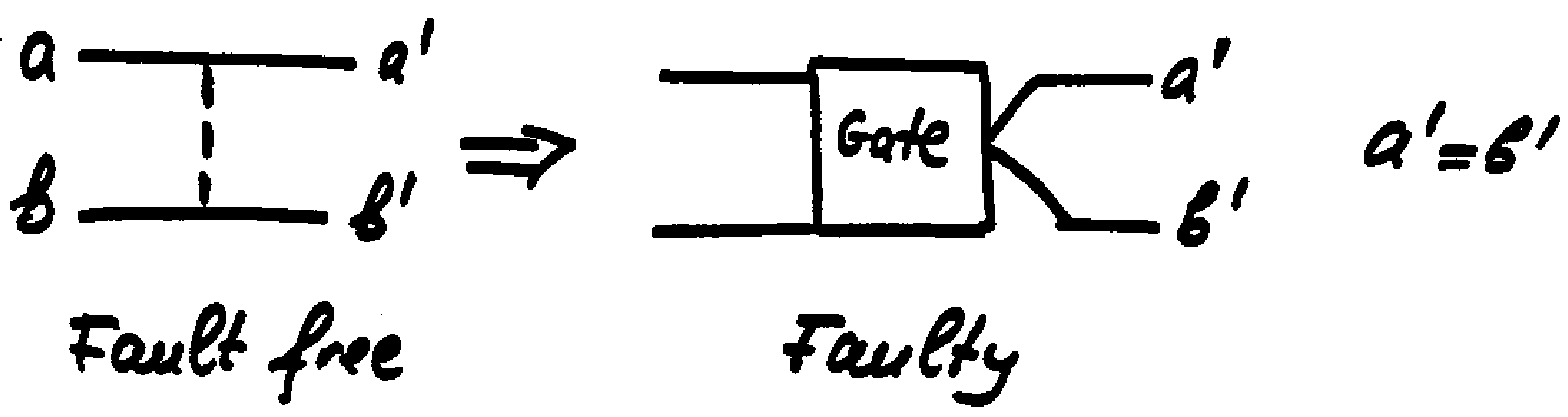
II Intermittent (transient, soft) faults

Detected only by on-line tests (ex. replication of hardware, parity checks, error-correcting codes, roll-backs of a program, etc.)

- Single intermittent faults (α-particles) vs repeating faults

- Up to 80% - 90% of faults are intermittent (Air Force, IBM)

III Bridgings (short circuits)
(high density of gates for VLSI)



∴ AND and OR type bridgings

AND: $(a, b)_*$

OR : $(a, b)_+$

a	b	AND $a' = b'$	OR $a' = b'$
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	1

Relation between stucks and bridgings:

$a/0 = (a, 0)_*$

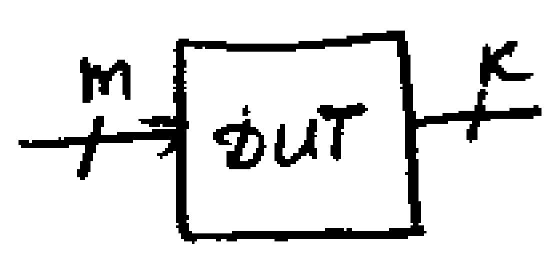
$a/1 = (a, 1)_+$

Number of bridgings:

$2 \binom{L}{2} = L(L-1)$

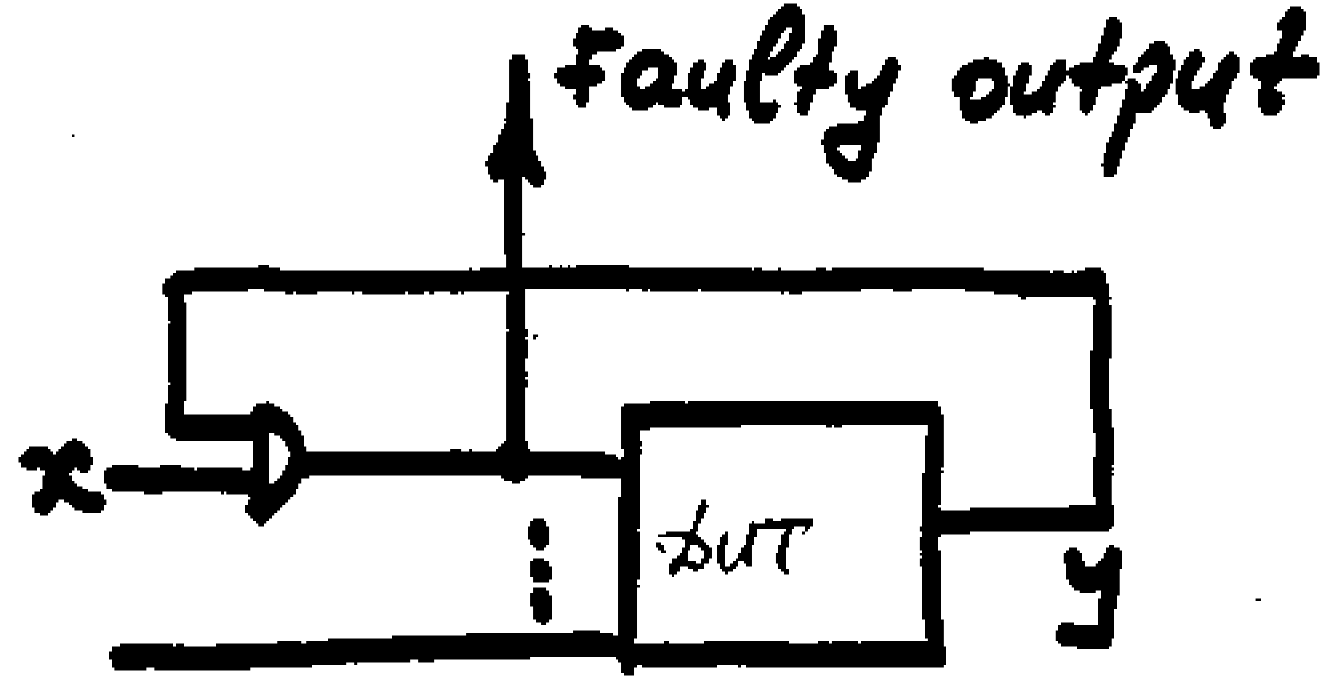
Feedback (FB) and NonFeedback (NFB) 1.8

Bridgings



$\Rightarrow$ m·k FB bridgings between inputs and outputs

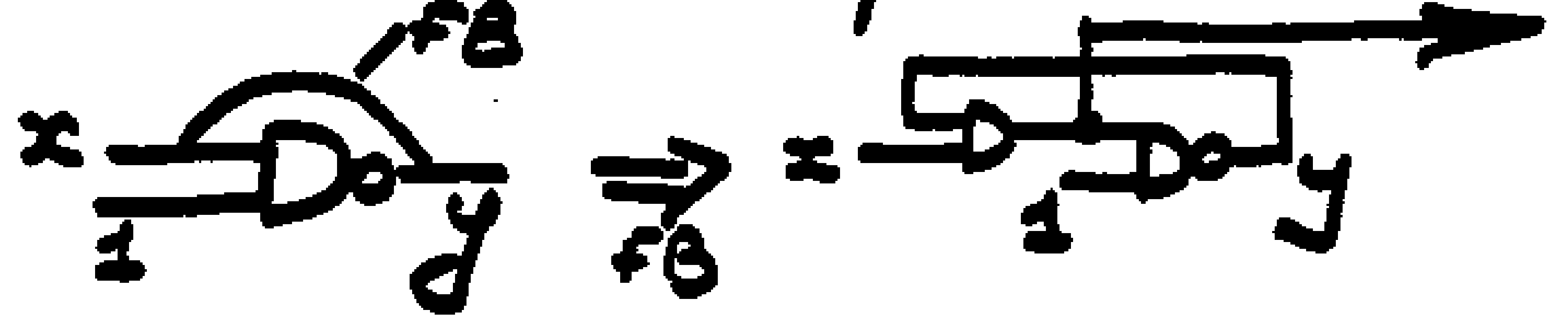
FB $(x,y)_*$



Combinational $\xrightarrow{FB}$ Sequential

Oscillation:

$(x,y)_*$

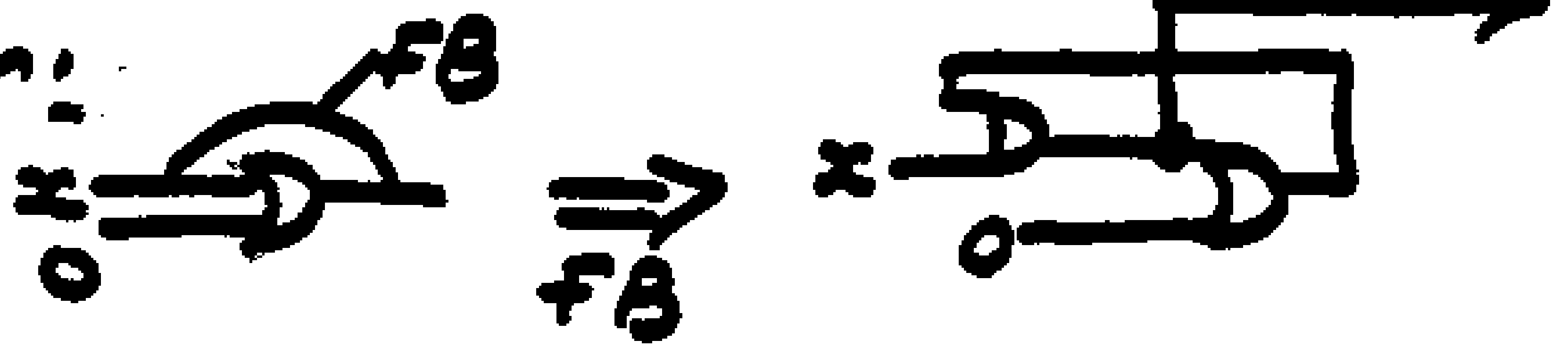


FOR x=1.

difficult to observe

Asynchronous Behavior:

$(x,y)_*$



(For any x output stay 0 after x=0 applied)

IV PLA Faults — CROSSPOINT FAULTS 1.10

1. A product term can grow (cover more minterms)

NOTATION: AG.

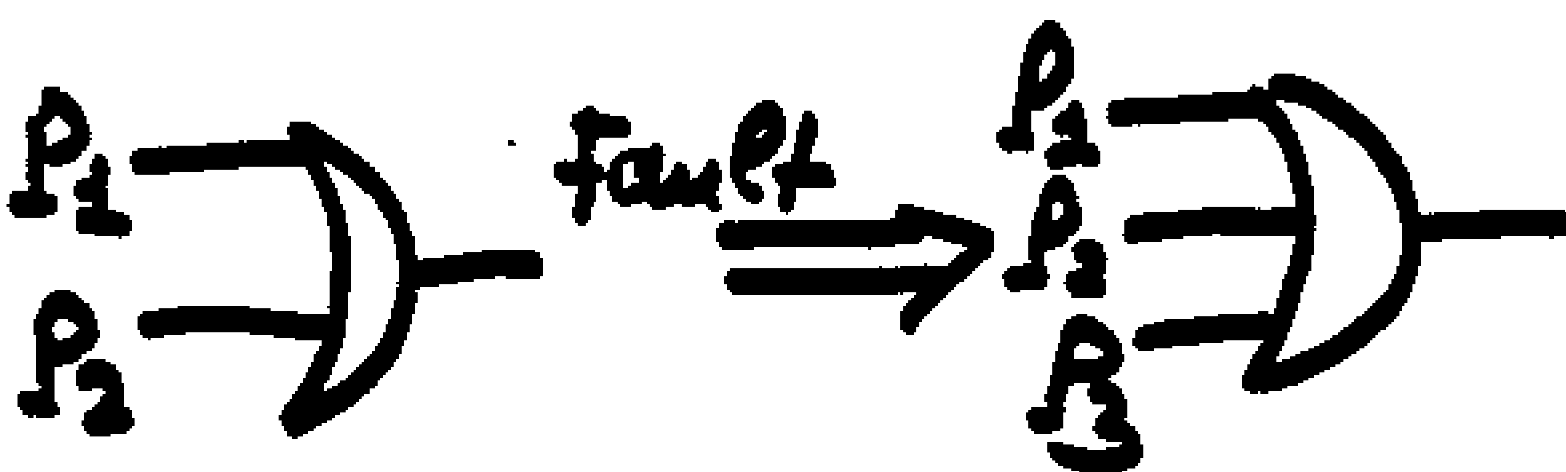
2. A product term can shrink (cover fewer minterms)

NOTATION: AS.

3. A product term can disappear from a function

NOTATION: OS

4. A product term from one function can appear also in another function



NOTATION: OG

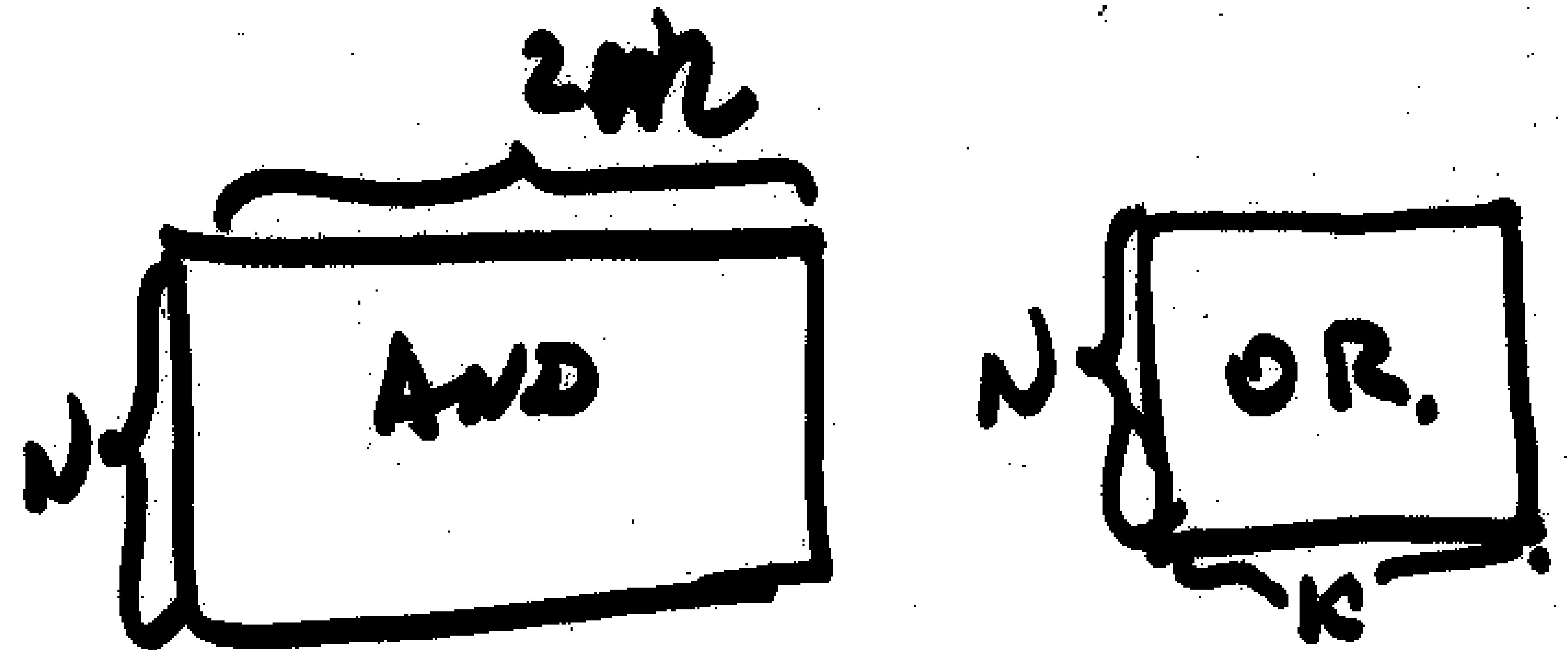
NUMBER OF CROSSPOINT

FAULTS

m - INPUTS

N - PRODUCT TERMS

K - outputs



$$2m \cdot N + NK = N(2m + K)$$

AND OR

RELATEVELY SMALL.

V Memory faults

5.1. Decoding errors
open decoder ⟹ no addressing
multiple writes, two addresses at a time
replacement of an address by another

5.2 INTERMITTENT FAULTS IN BINARY CELLS

5.2'. Stuck-at faults in binary cells

5.3. Bridgings between cells

5.4 Bursts on a surface of a disc or tape

For semiconductor memories:

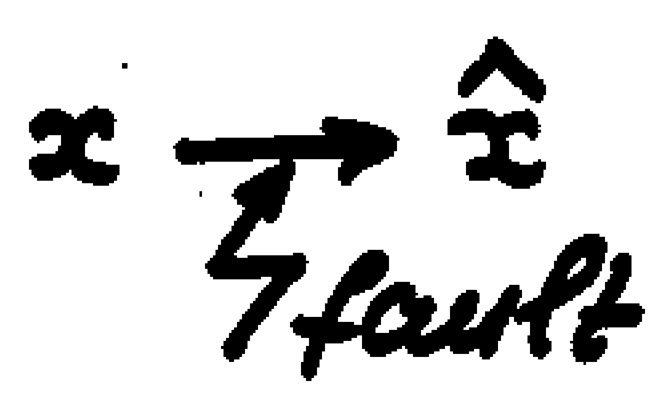
5.5 Hold time for refreshing data ⟹
sleeping sickness - graceful degradation of performance

5.6. Write recovery - not producing data at a given access time if each READ is preceded by WRITE

TIME FAULTS

IV Arithmetical Faults (ALU)

Typical for adders, subtractors counters, multipliers, etc.



Multiplicity l: $|x-\hat{x}| = \pm 2^{i_1} \pm \quad \pm 2^{i_l}$

Example: $x = 0111$, $\hat{x} = 1000 \Rightarrow l = 1$
(For stuck-at fault model $l = 4$)

Number of faults: $\sum_{i=1}^{l} 2^i \binom{m}{i}$ - symmetrical
m- number of bits $\sum_{i=1}^{l} \binom{m}{i}$ - uniderctional

Symmetric, asymmetric and unidirectional arithmetical faults

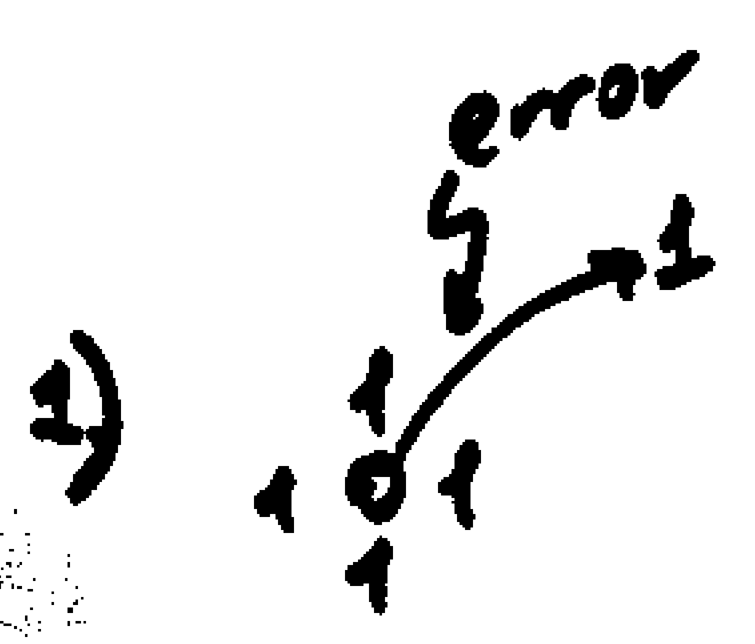
Arithmetical codes (modulo A checks)

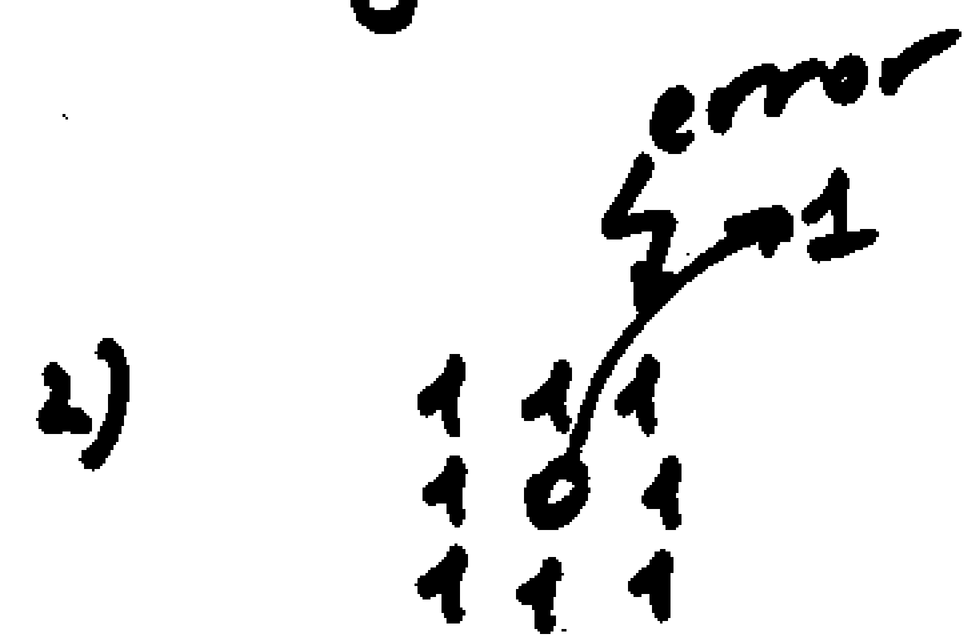
Example $l = 1 \Rightarrow A = 3$ TO DETECT SINGLE SYMMETRICAL ARITHM. ERRORS.

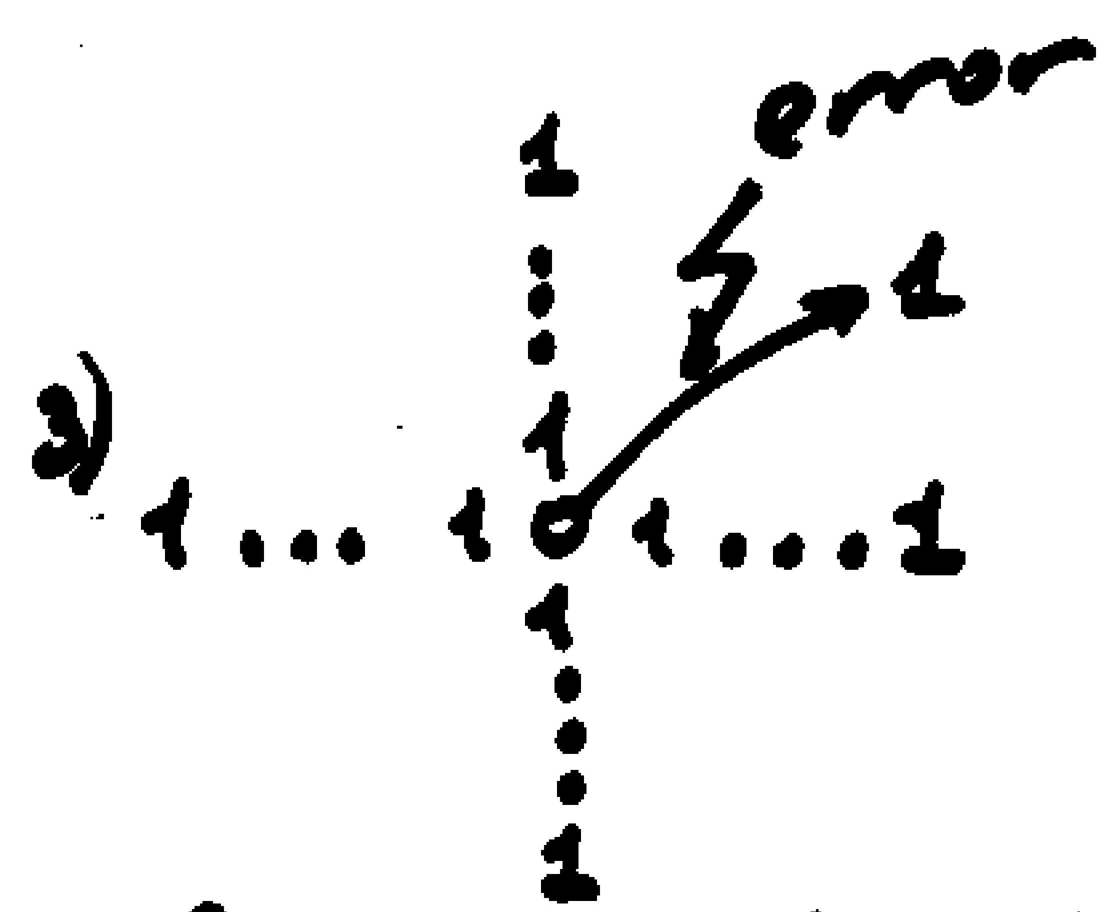
5.7. Pattern-sensitive faults (crosstalks) –

impossible to write 0 (1) surrounded by 1's (0's)

Electrical neighbourhoods

1) 

2) 

3) 

These faults are most difficult to test

Testing time (test complexity, number of READ and WRITE operations) is proportional to the size of a neighbourhood

VII Functional Faults (µprocessors)

7.1. Replacement of one instruction I_i by another I_j, I_i/I_j

7.2. Replacement of an instruction I_i by no instruction, I_i/ϕ

7.3 Replacement of an instruction I_i by two instructions I_j and I_k, I_i/I_j+I_k

These faults are detected by functional testing (function verification)

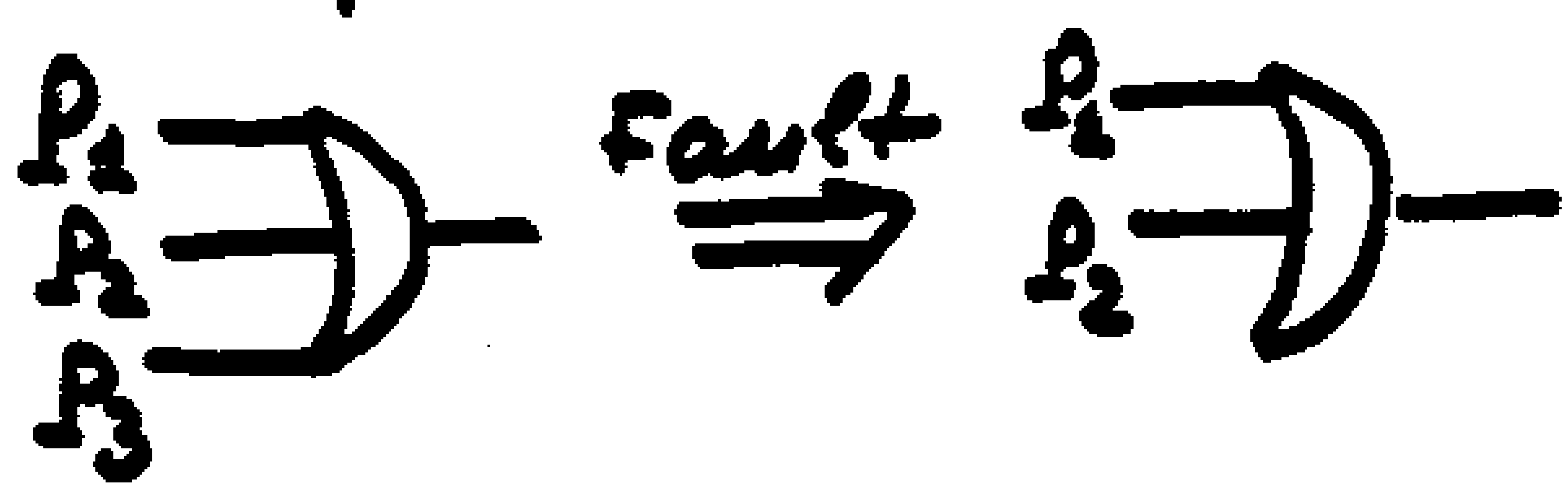
DEVICE ORIENTED FAULT MODELS

V PLA Faults

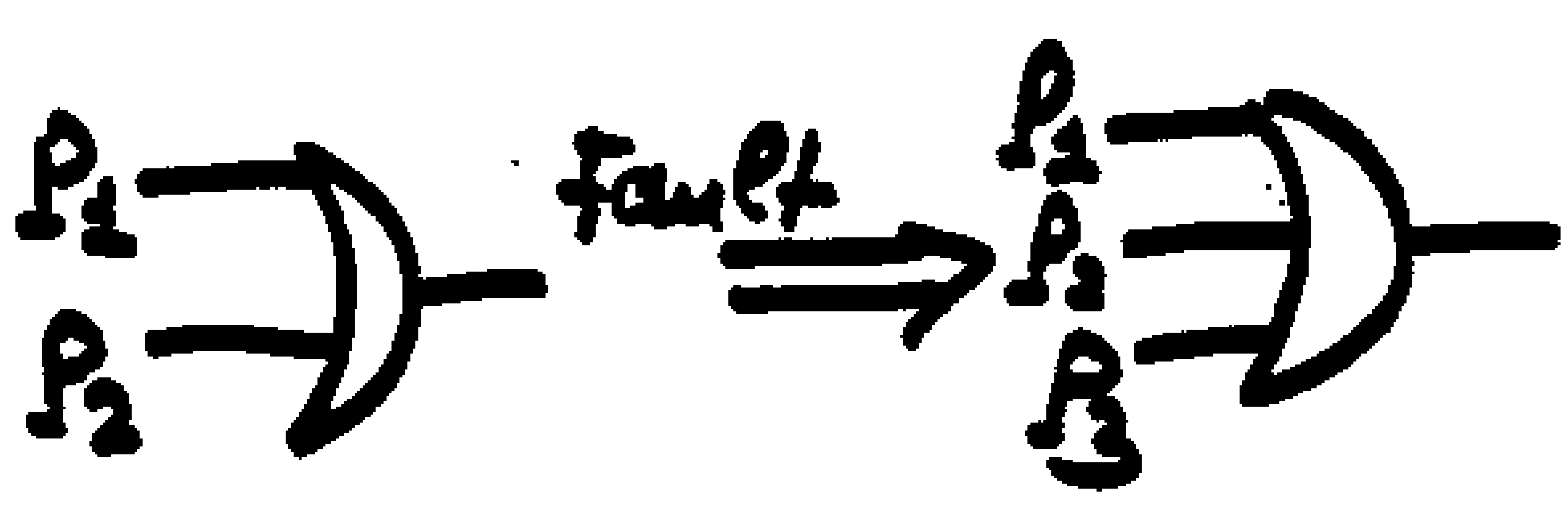
1. A product term can grow (cover more minterms)

2. A product term can shrink (cover fewer minterms)

3. A product term can dissappear from a function



4. A product term from one function can appear also in another function



VI Memory faults

$l=1$ UNIDIRECTIONAL

5.1. Decoding errors

open decoder ⇒ no addressing

multiple writes, two addresses at a time

replacement of an address by another

$l=2$ SYMMETRICAL

5.2. Stuck-at faults in binary cells

5.3. Bridgings between cells

5.4 Bursts on a surface of a disc or tape

For semiconductor memories:

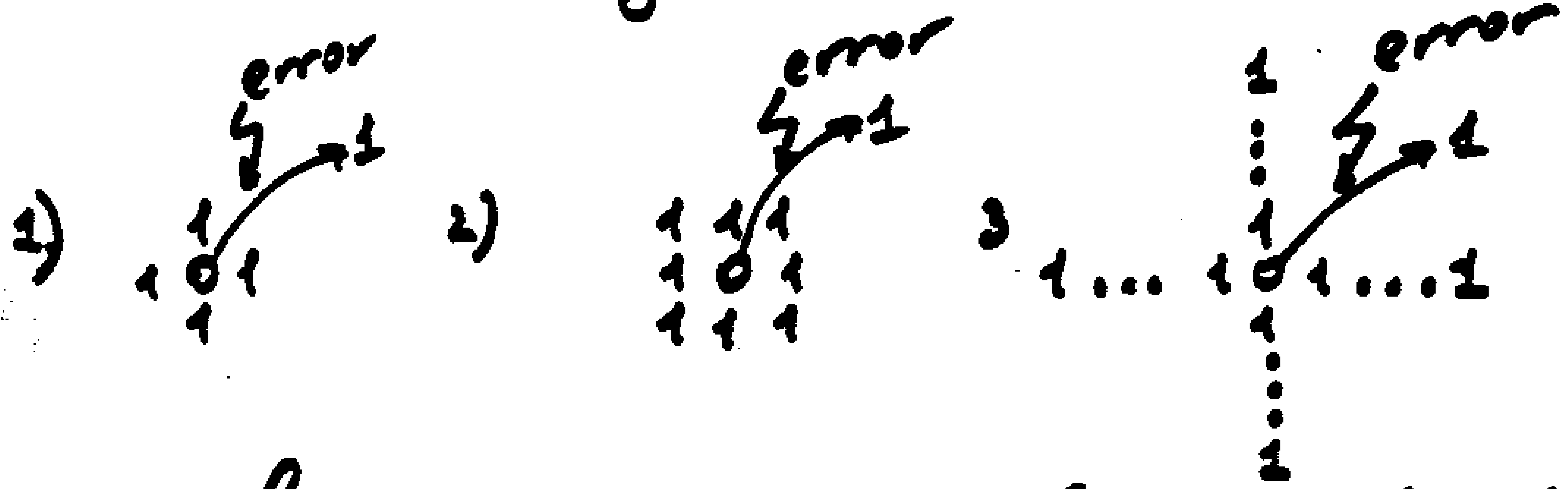
5.5 Hold time for refreshing data ⇒
sleeping sickness - graceful degradation of performance
(for dynamic memories)

5.6. Write recovery - not producing data at a given access time if each READ is preceded by WRITE

5.7. <u>Pattern-sensitive faults</u> (<u>crosstalks</u>) –
impossible to write 0 surrounded by 1's

<u>STATIC</u>

<u>Electrical</u> <u>neighbourhoods</u>



these faults are most difficult to test

<u>Testing time</u> (test complexity, number of READ and WRITE operations) is proportional to the size of a neighbourhood

DYNAMIC PATTERN SENSITIVE FAULTS

COUPLING

TWO- COUPLINGS

1. <↑,↓> ⇒ 0→1 TRANSITION IN CELL i results in setting CELL j into 0 from 1
2. <↑,↑> ⇒ 0→1 in cell i results in setting cell j into 1. from 0
3. <↓,↓> ⇒ 1→0 in i sets j into 0 from 1

CHANGES IN MEMORY PATTERNS RESULTS IN FAULTS

4\. $\langle \downarrow, \uparrow \rangle \Rightarrow$ $1 \rightarrow 0$ in i sets j into 1 from 0

5\. $\langle \uparrow, \updownarrow \rangle \Rightarrow$ $0 \rightarrow 1$ transition in cell i results in negation of a content of cell j

6\. $\langle \downarrow, \updownarrow \rangle \Rightarrow$ $1 \rightarrow 0$ in i results in negation of contents of j

<u>K-couplings</u> ⇒ couplings between two cells with a neighbourhood of K cells when remaining K-2 cells are in a certain state

<u>Ex</u> (↓ 0 0 0 ↓) (K=5)

(↓,↓) coupling between cells 1 and 5 when cells 2,3,4 are 000.

VII Functional Faults (μprocessors)

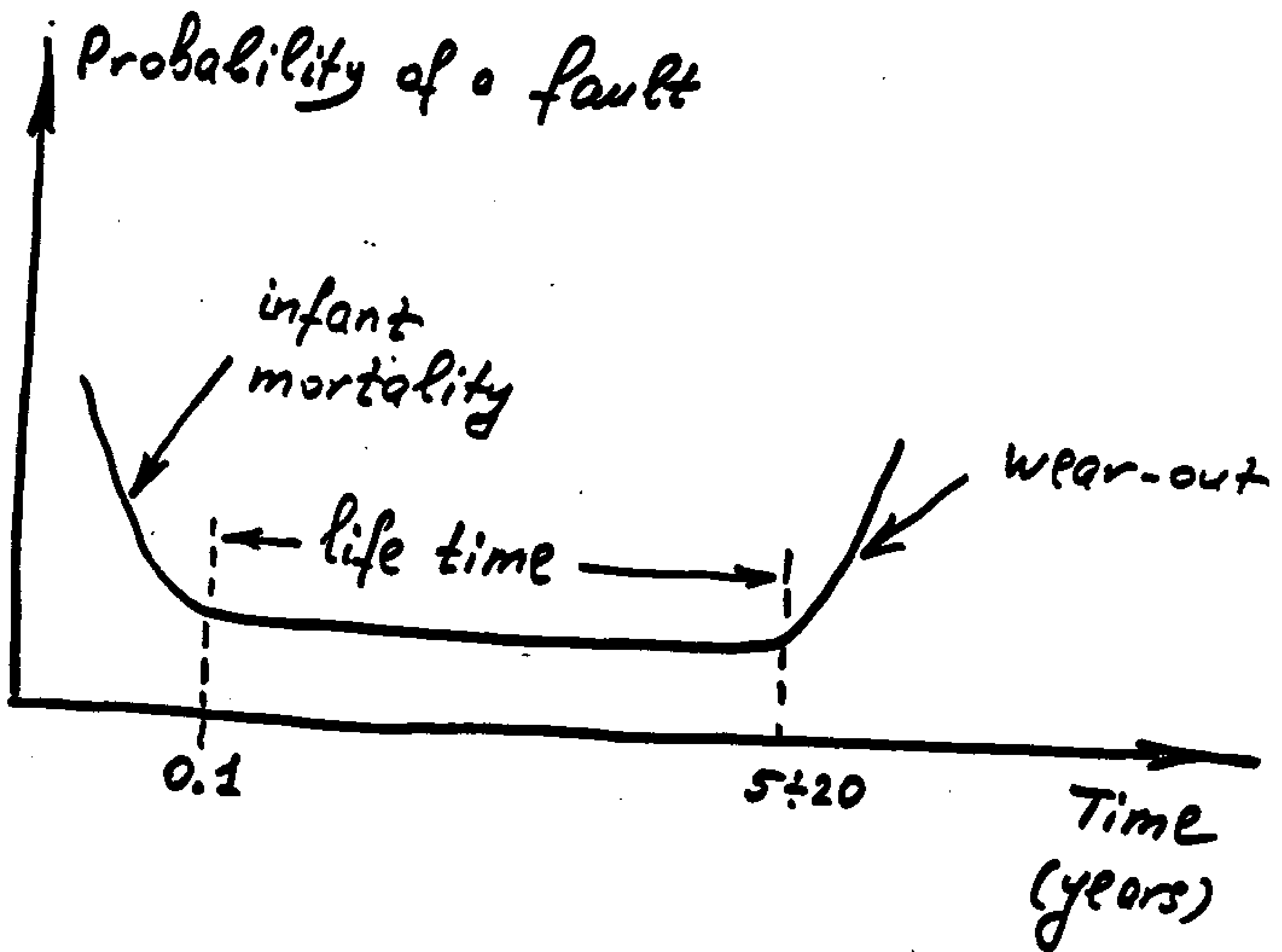
7.1. Replacement of one instruction I_i by another I_j, I_i/I_j

7.2. Replacement of an instruction I_i by no instruction, $I_i/\emptyset$

7.3 Replacement of an instruction I_i by two instructions I_j and I_k, $I_i/I_j + I_k$

These faults are detected by functional testing (function verification)

Fault model may <u>depend on time</u>



VIII. Network faults

Faults in distributed systems

8.1. Node faults

Multiplicity of a node fault = number of processors in the system which are faulty at the same time

8.2. Link faults

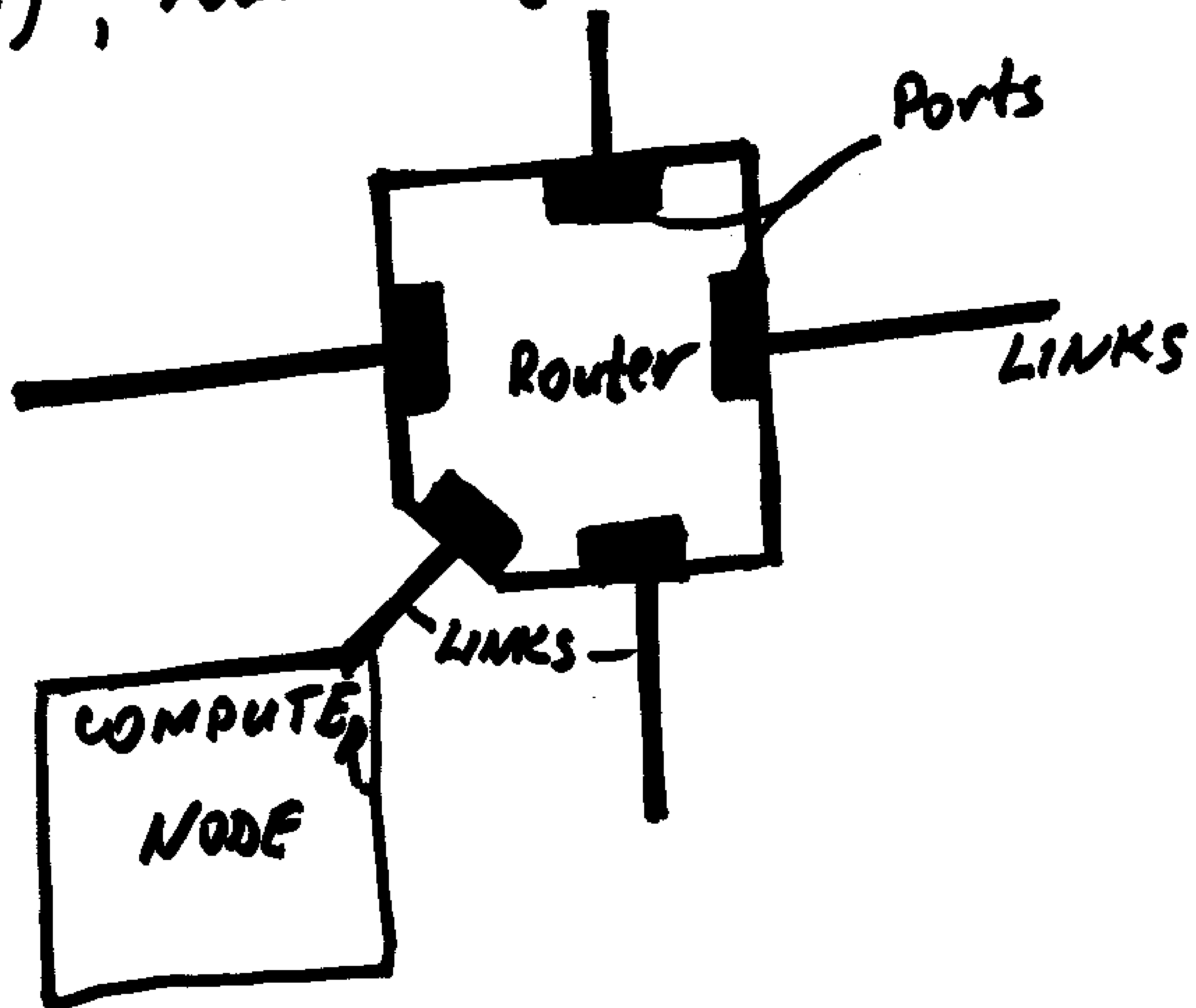
Multiplicity of a link fault = number of links between nodes which a faulty at the same time.

∴ Optimal test strategy for a given topology of links.

∴ Optimal topology of links for a given class of faults.

ROUTER FAULTS IN COMPUTER AND COMMUNICATION NETWORKS AND MULTIPROCESSORS

Networks consist of computing nodes (with processor, RAM, ROM, bus), routers (switches) and links.



- **TOTAL ROUTER FAULTS**

  (NO CONNECTION BETWEEN INPUT AND OUTPUT PORTS)

- **PARTIAL ROUTER FAULTS**

  (NO CONNECTION FOR ONE PAIR OF INPUT-OUTPUT PORTS; e.g. message cannot be send from a horizontal to a vertical link)

GENERAL ERROR MODELS AT THE CHIP LEVEL

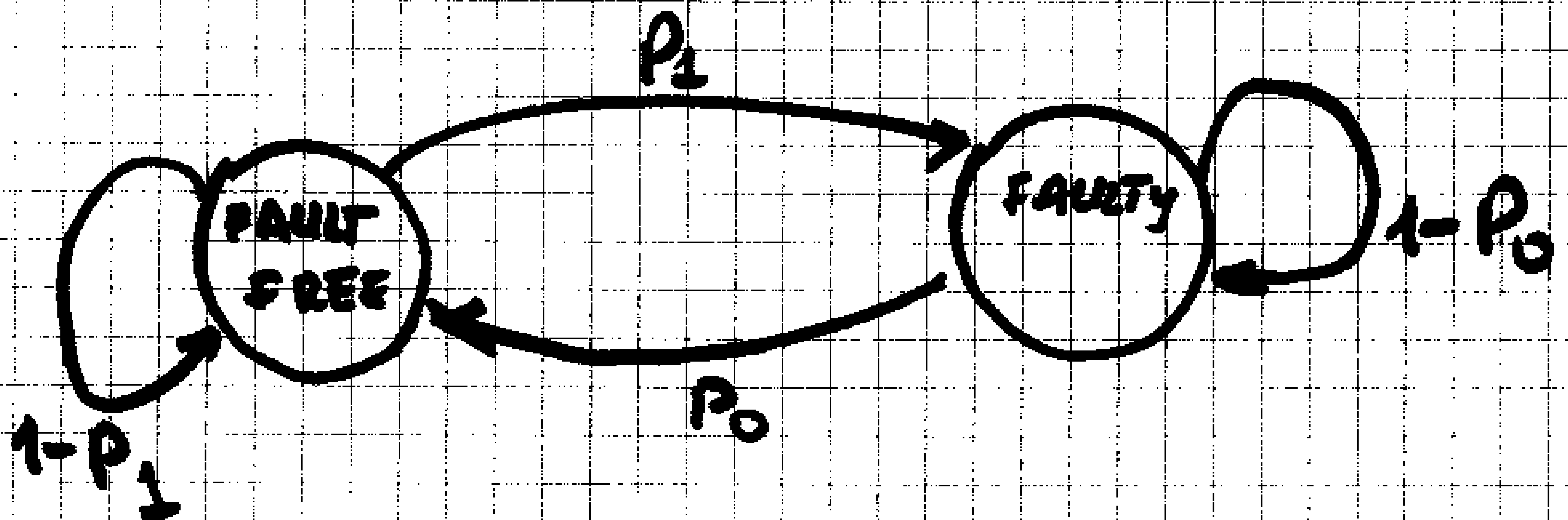
∴ TEMPORAL AND SPATIAL COMPONENTS OF ERROR MODELS

∴ FOR COMBINATIONAL DEVICES AND COMBINATIONAL FAULTS ALL ERRORS ASSUMED TO BE TIME-INDEPENDENT

TIME CORRELATED ERROR MODELS

(MARKOV CHAIN MODELS)

(P_0, P_1 - model)



P_1 = Prob that the device is fault-free at clock t and faulty at clock $t+1$

P_0 = Prob that the device is faulty at clock t and fault-free at clock $t+1$.

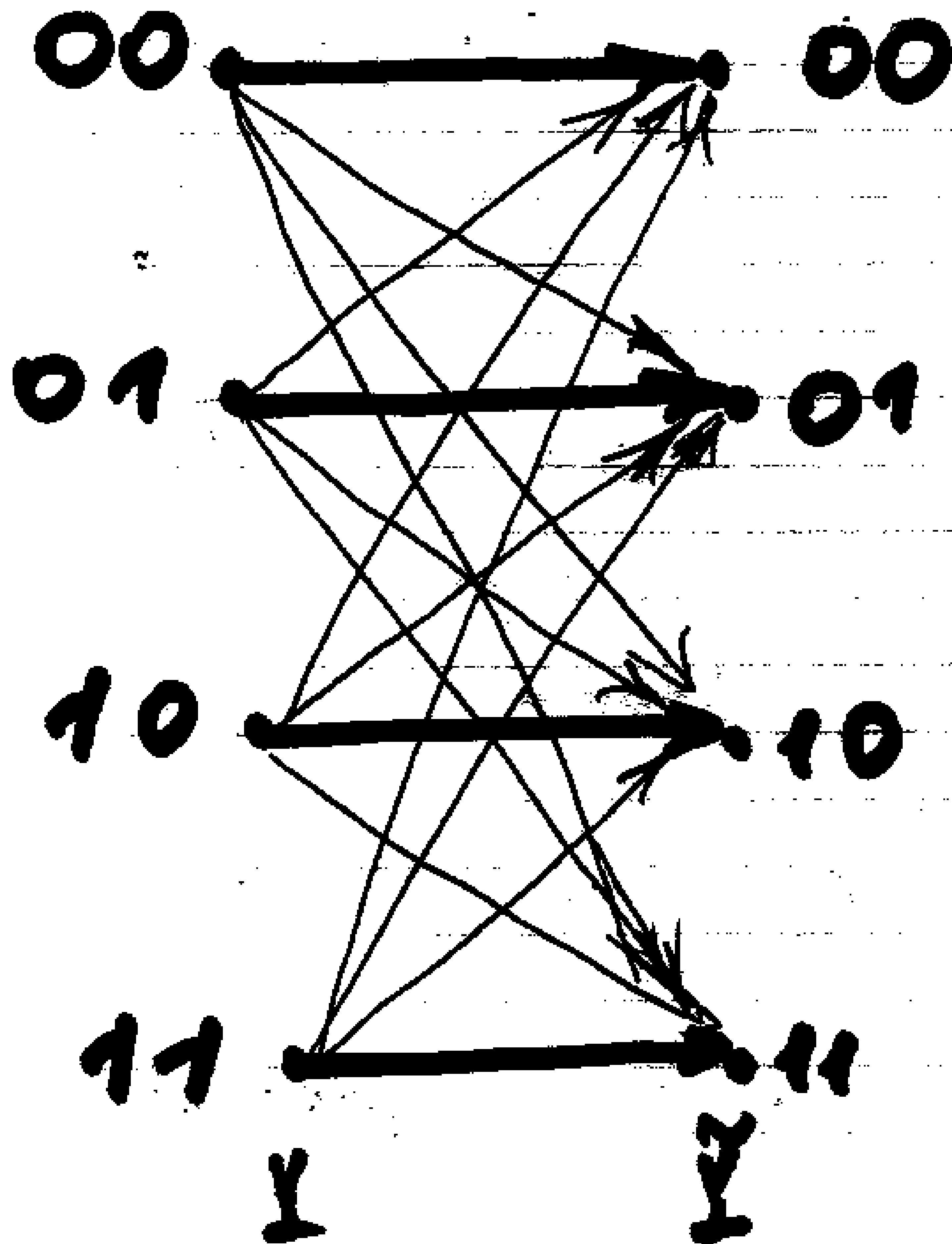
SPATIAL ERROR MODELS

1. q-ary symmetrical model

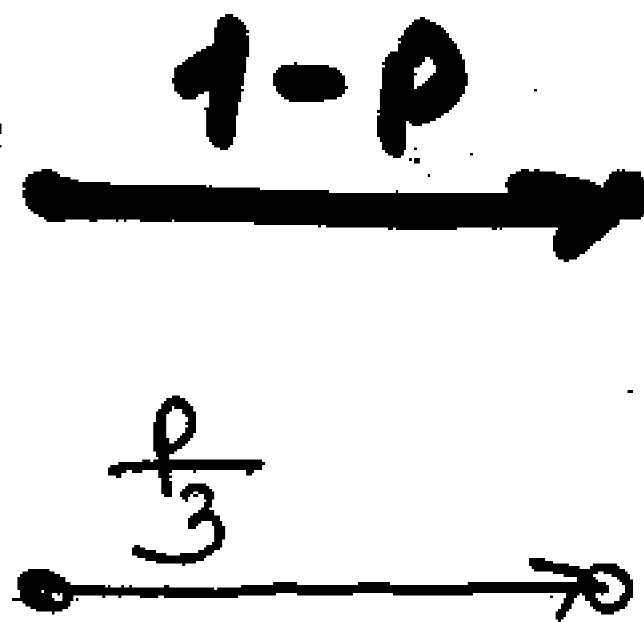
For a device with m output lines let $q=2^m$

We assume all $q-1$ possible distortions at any given time being equiprobable

EXAMPLE : $m=2$ $q=4$
symmetrical



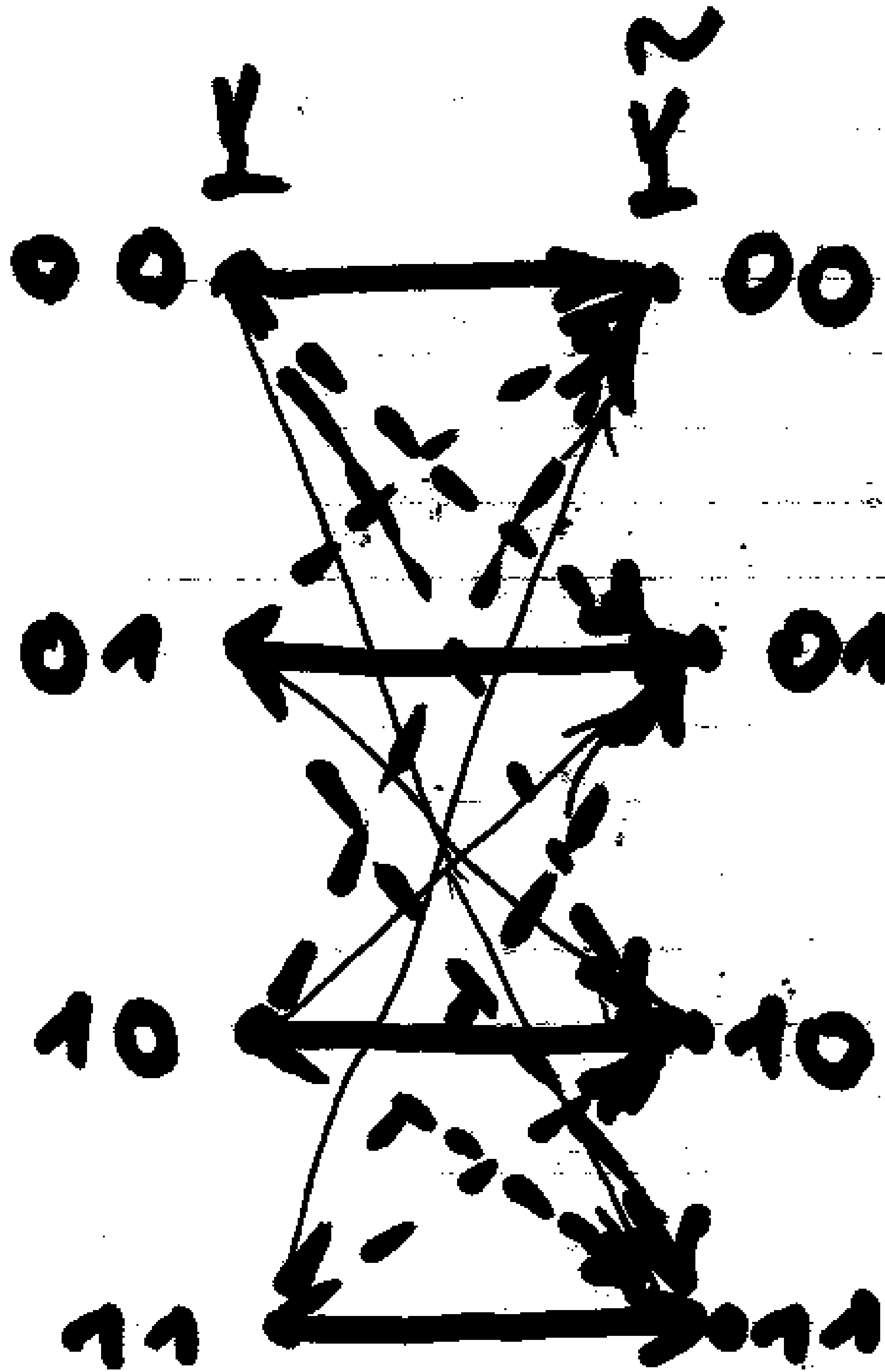
4 ARY
SYMMETRICAL
CHANNEL



2. INDEPENDENT ERRORS

DISTORTION OF EXACTLY
n out of m output bits
happens with probability
$p_b^n (1-p_b)^{m-n}$ at <u>any moment</u>
where p_b is a probability
of a distortion in
one bit.
(bit distortion rate)

EXAMPLE: $m=2$ $q=4$ INDEPENDENT ERRORS



4ary independent channel

$1-p_b^2-2p_b$

$p_b(1-p_b)$

p_b^2

3. General space model

General error model is defined by error distribution

$p_0, p_1, \ldots, p_{q-1}$

where $p_i = \text{Prob}\{e = i\}$

$e = y \oplus \tilde{y}$ — FAULTY OUTPUT

FAULT FREE OUTPUT

FOR MOST CASES:

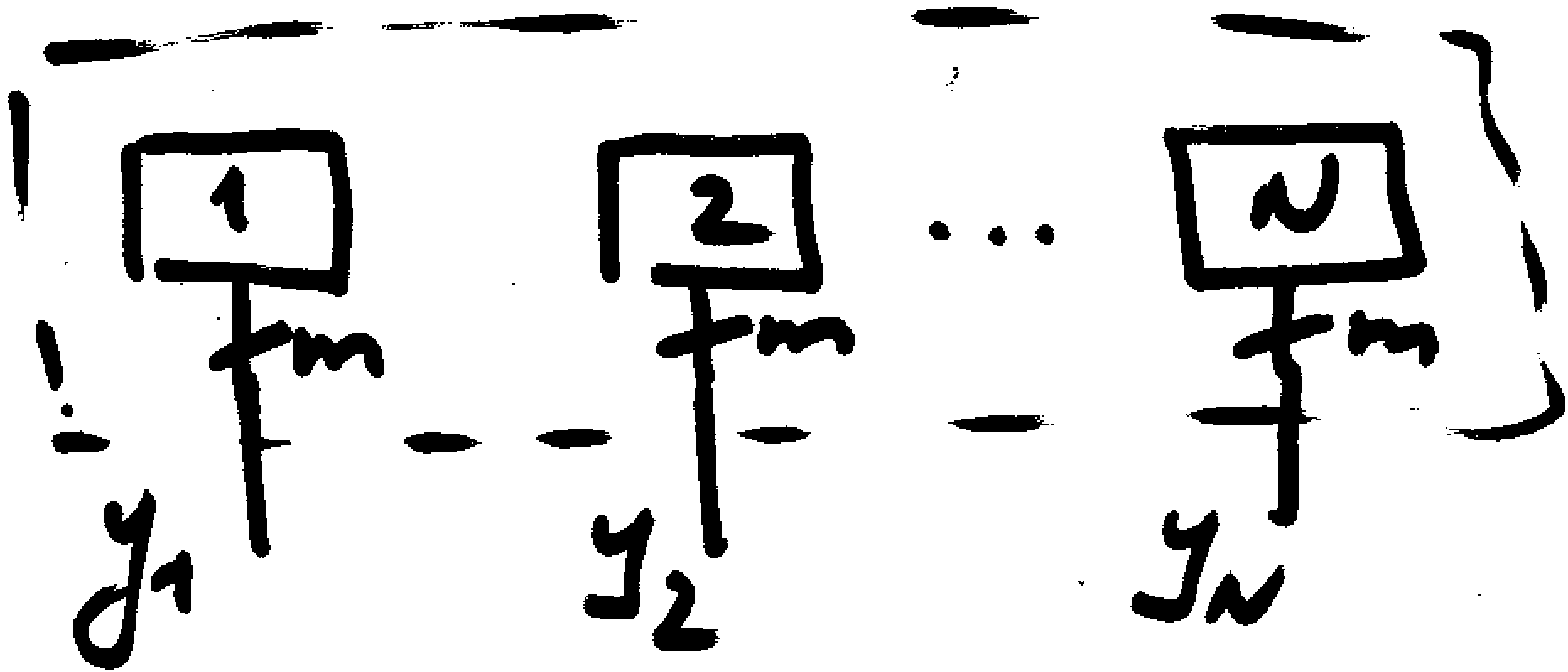
1. INDEPENDENT MODEL IS PESSIMISTIC

2. SYMMETRICAL MODEL IS OPTIMISTIC

KARPOVSKY, GUPTA, PRADHAN "ALIASING AND DIAGNOSTIC PROBABILITY IN MISR..." Proc. INT TEST CONF. 1991 pp 828 - 840.

ERROR MODELS AT THE SYSTEM LEVEL.

CONSIDER A SYSTEM WITH N COMPONENTS (CHIPS)



1. <u>CHIP-INDEPENDENT</u> MODELS

ERRORS IN DIFFERENT CHIPS ARE INDEPENDENT.

INSIDE A CHIP ERRORS ARE DISTRIBUTED ACCORDING TO ONE OF THE CHIP MODELS (INDEPENDET, SYMMETRICAL ORE GENERAL)

2. System-dependent ERRORS (FOR ARRAY PROCESSORS, MESHES)

correlated errors

EXAMPLE

WE HAVE THE FOLLOWING EQUIPROBABLE ERRORS (GENERATED BY SINGLE FAULTY NODES)

$(e_1, e_2, 0, 0)$, $(e_1, e_2, e_3, 0)$, $(0, e_2, e_3, e_4)$

$(e_2, e_3, 0, 0)$, $(0, 0, e_3, e_4)$

$(e_1, 0, 0, 0)$, $(0, e_2, 0, 0)$, $(0, 0, e_3, 0)$, $(0, 0, 0, e_4)$

$e_1, e_2, e_3, e_4 \in \{01, 10, 11\}$.

IV Arithmetical Errors (ALU)

Typical for adders, subtractors counters, multipliers, etc.

$$x \xrightarrow[\text{fault}]{} \hat{x}$$

Multiplicity l: $|x-\hat{x}| = \pm 2^{i_1} \pm \quad \pm 2^{i_l}$

Example: $x = 0111$, $\hat{x} = 1000 \Rightarrow l = 1$
(For stuck-at fault model $l = 4$)

Number of Errors: $\sum_{i=1}^{l} 2^i \binom{m}{i}$ - symmetrical

m- number of bits $\sum_{i=1}^{l} \binom{m}{i}$ - uniderctional

Symmetric, asymmetric and unidirectional arithmetical faults

Arithmetical codes (modulo A checks)

Example $l = 1 \Rightarrow A = 3$ (DETECTION)

ARITHMETICAL BURSTS OF LENGTH b

$$|x-\hat{x}| = c_1 2^{i_1} + c_2 2^{i_1+1} + \ldots + c_b 2^{i+b-1}$$

$c_i \in \{-1, 0, +1\}$ symmetrical

$c_i \in \{0, 1\}$ – unidirectional

$c_i \in \{-1, +1\}$ – solid