Testing Strategies

Off-line testing

0. Selecting FAULT (ERROR) MODELS
I. Test generation

complexity of test generation (TGT) ↑

- Gate-level – (GT)
- Functional – (FT)
- Universal (UT)
- Random (RT)
- Exhaustive (ET)

↓ Length of a test (testing time) (TL)

RANDOM (PSEUDORANDOM) TESTS MAY BE UNBIASED AND BIASED.

Comparison of test generation strategies

Input data:

GT - gate-level description of DUT and faults F

FT - functional description of DUT and F

UT - functional description of F

RT, ET - parameters (# of I/O pins, etc) of DUT

Test Generation Time (TGT)

$$TGT(GT) \geq TGT(FT) \geq TGT(UT) \geq TGT(RT) \geq TGT(ET)$$

Test length (TL), Testing Time

$$TL(GT) \leq TL(FT) \leq TL(UT) \leq TL(RT) \leq TL(ET)$$

UNIVERSAL TESTING

	FUNCTIONAL TEST	UNIVERSAL TEST	RANDOM . TEST
INPUT FOR TEST GENERATION	FUNCTIONAL DESCRIPT. OF: 1) A DUT 2) A CLASS OF FAULTS	DECRIPTION OF FAULTS	DECRIPTION OF A CLASS OF DEVICES

UNIVERSAL TESTING ⇒ STANDARD DETERMINISTIC TEST FOR A CLASS OF DEVICES FOR A GIVEN FAULT MODEL.

FAULT-ORIENTED

⇒ GOOD ON AVERAGE

⇒ EFFICIENT FOR MOST OF THE DEVICES

FRACTION OF DEVICES SUCH THAT OUR UNIVERSAL TEST is EFFICIENT is growing (TO 1) as THE SIZE OF THE DEVICE is GROWING.

1) VLSI devices

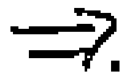
2) broad spectrum

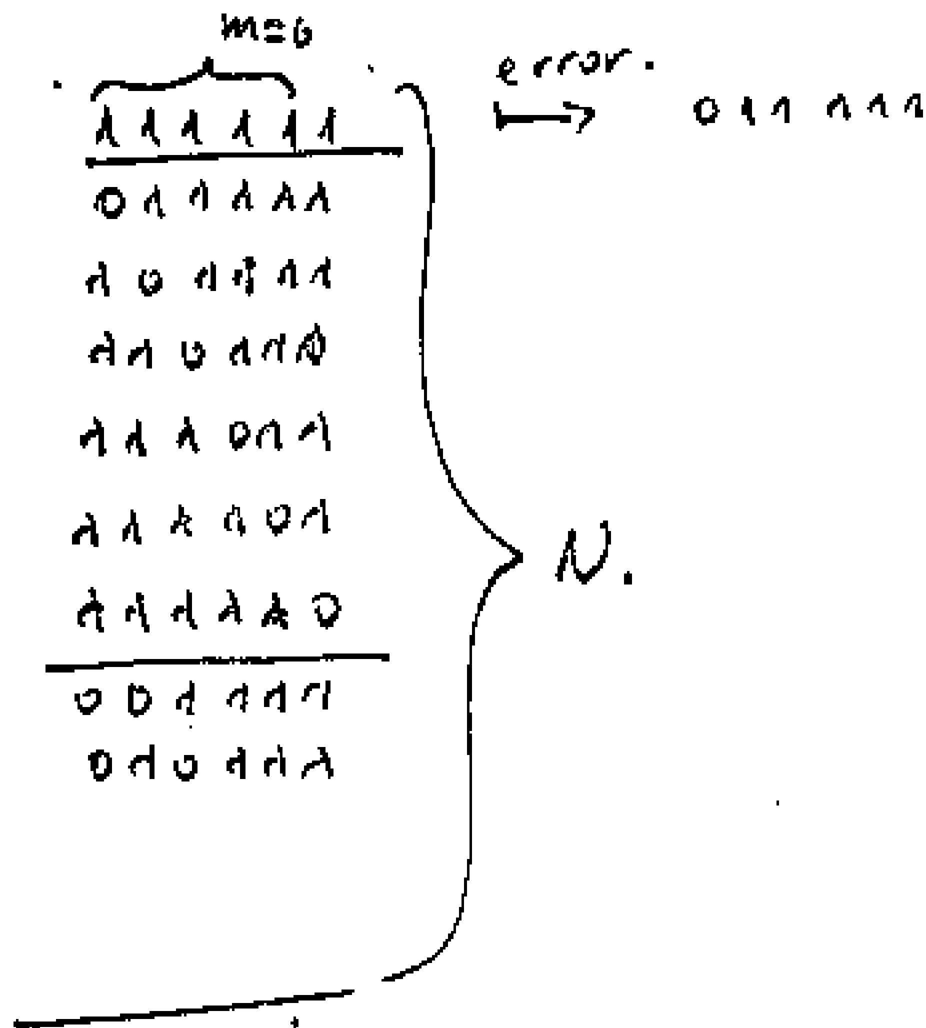
3) can TOLERATE A SMALL FRACTION α OF CASES WHEN UNIVERSAL TESTS ARE NOT EFFICIENT ($\alpha \to 0$ if $m \to \infty$)

FOR A CLASS OF FAULTS $\longrightarrow$ UNIVERSAL TEST

S/0 AT INPUT LINES

UNIVERSAL TEST OF LENGTH N





II. Observation of test responses

1. "Golden copy" approach
2. Stored response approach
3. Simulation

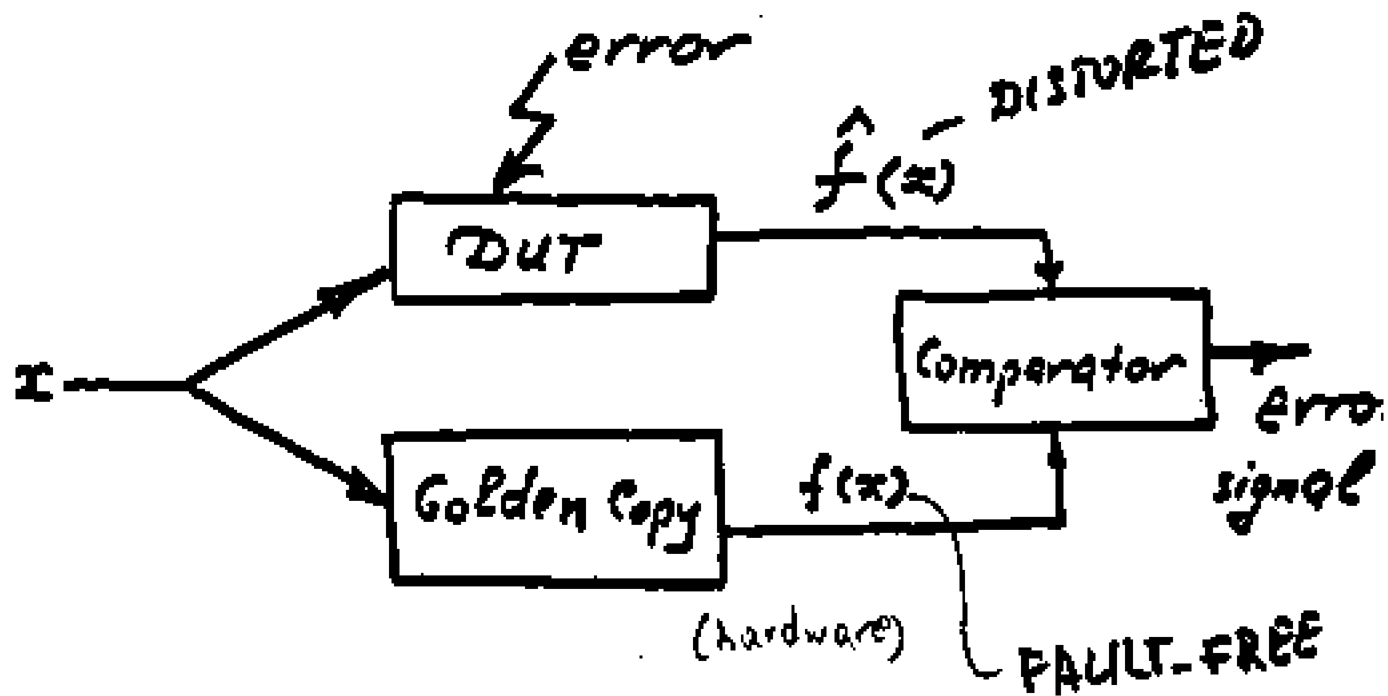
Approaches 1,2,3 are very expensive

4. Data compression of test responses

Signature analysis

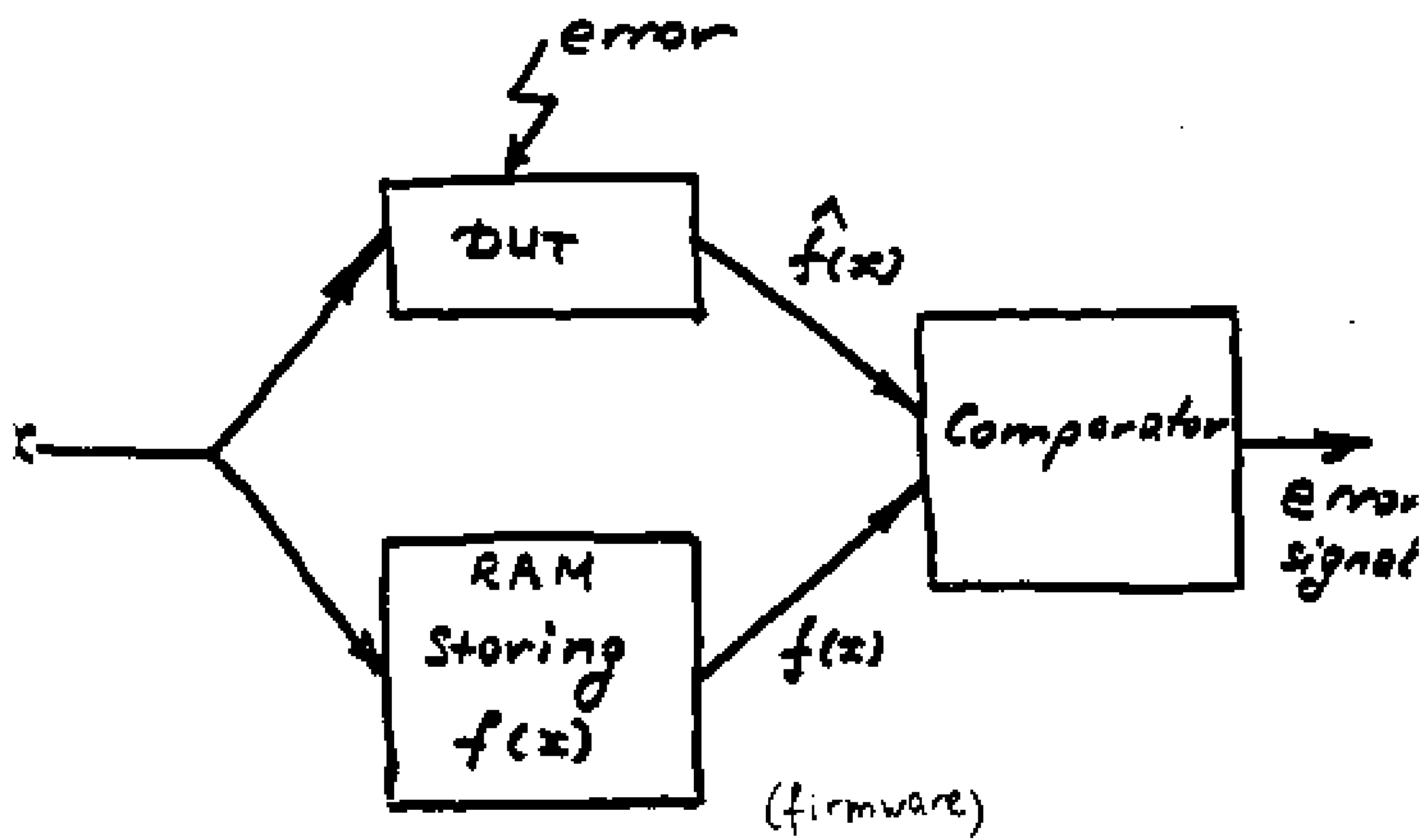
Linear Feedback Shift Registers

"Golden Copy" Approach



FOR THE CASE WHEN MANY COPIES OF THE SAME device

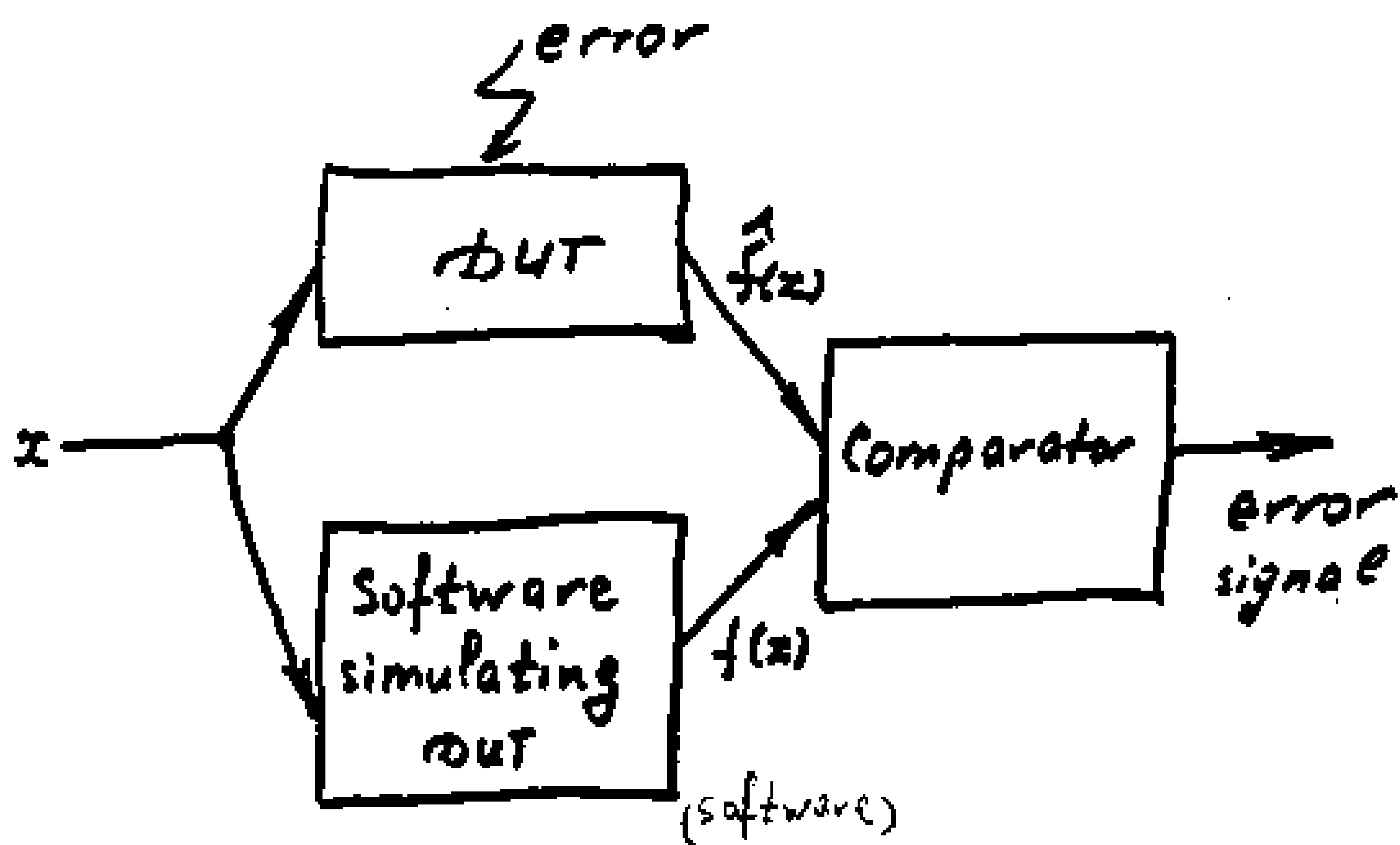
Stored Response Approach



Advantage: FLEXIBILITY

Limitation: TEST OBSERVATION

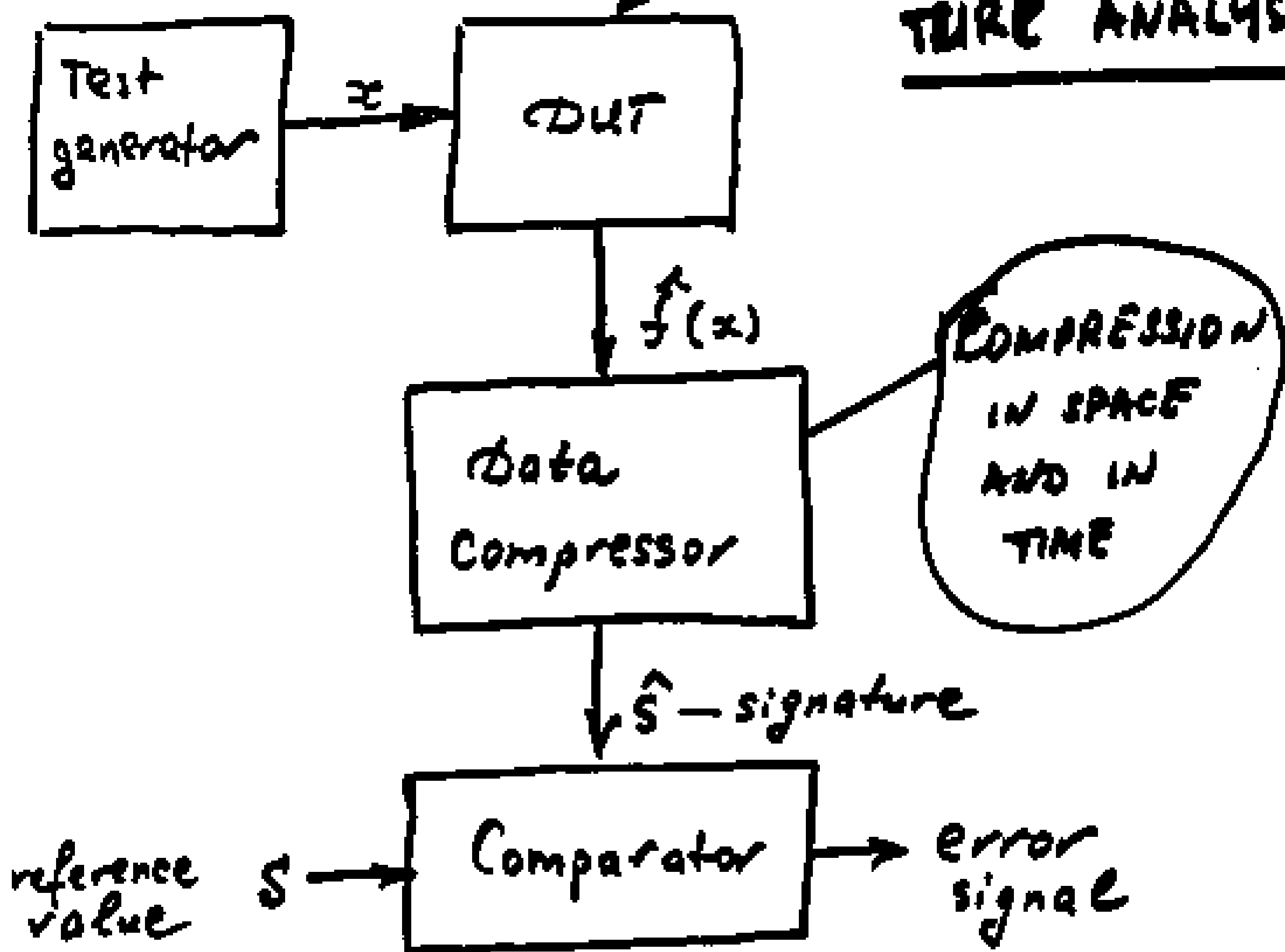
Simulation



$f(x)$ - reference value

Simulators are very expensive and slow

Data Compression of Test Responses



$\hat{S}$ - signature (syndrome) of an error

S - signature of a fault-free device

Testing Strategies

III. On-line testing (Self-test, built-in-test)

Hardware redundancy (replication with voting)

Information redundancy (parity checks on buses, error-correcting codes in memories, etc)

Time redundancy (rollback procedures)

Error masking (error correction)

Tradeoffs between off-line and on-line testing

∴ on-line testing is the only way to detect intermittent faults

IV. DESIGN FOR TESTABILITY