SC 752 – Computer Hardware Testing

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SC-752 LECTURE TOPICS

Title

- ➔ Introduction to Testing
- ➔ Test Economics
- ➔ Testing and Design Verification
- ➔ Fault Models
- ➔ Error Models
- ➔ Test Strategies
- ➔ Gate-level Testing
- ➔ Detection of Bridging Faults
- ➔ Testing by Boolean Differences
- ➔ Detection of Multiple Faults
- ➔ Testing of Special Classes of Devices
- ➔ Functional Testing
- ➔ Pseudoexhaustive Testing
- ➔ Memory Testing
- ➔ Testability Analysis
- ➔ Random Testing
- ➔ Data Compression of Test Responses
- ➔ Design for Testability
- ➔ Board Level Diagnosis
- ➔ Robust compression of test responses
- ➔ Built-in Self Diagnosis
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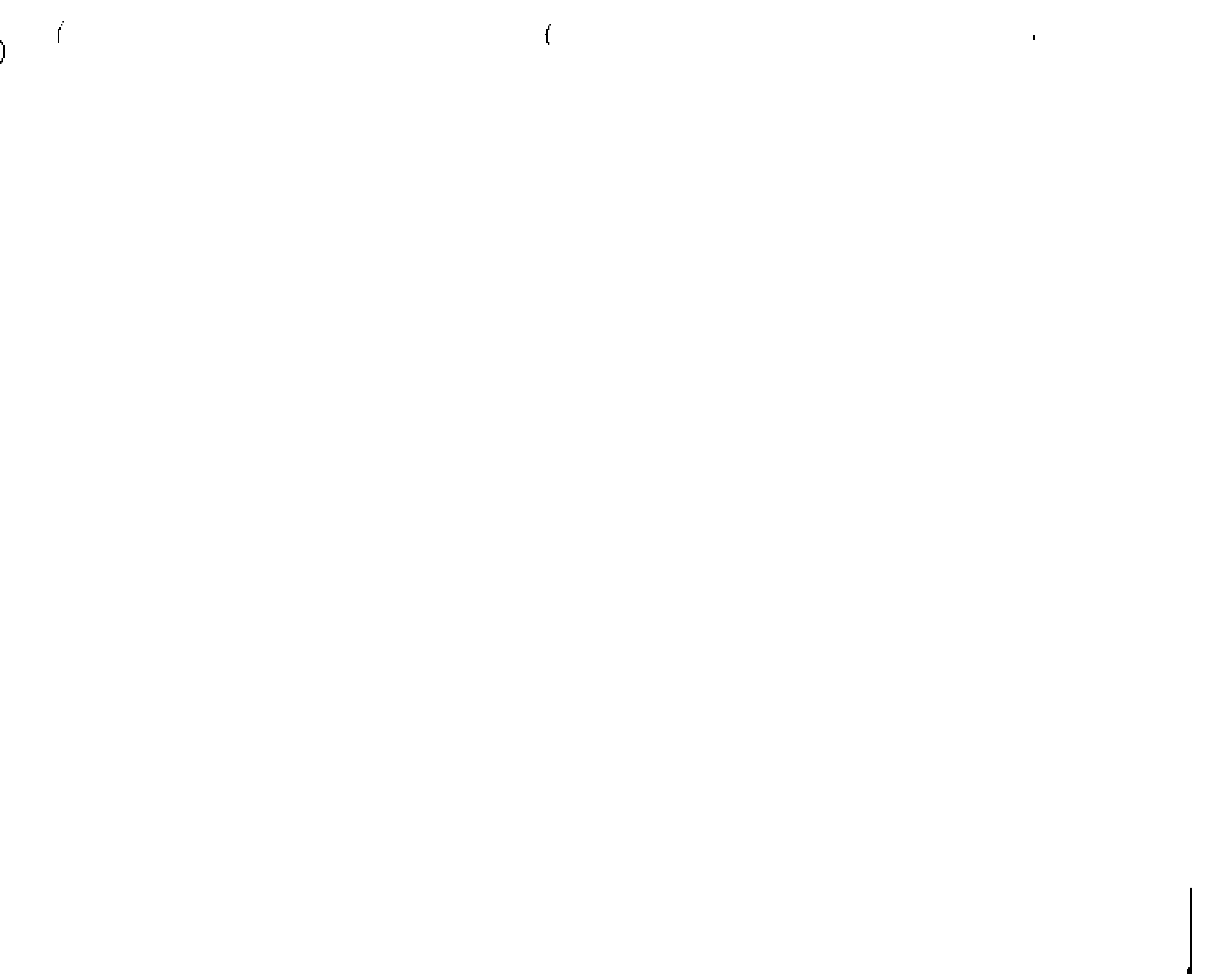


- $130 billions sales in semiconductor industry
- 50% increase in sales of testing equipment
- $25 billions cost of testing

testing is the largest expense item in semiconductor fabrication process!

Cost of Testing

For complex devices

cost of testing > cost of design and manufacturing

Testing is a bottleneck in computer industry

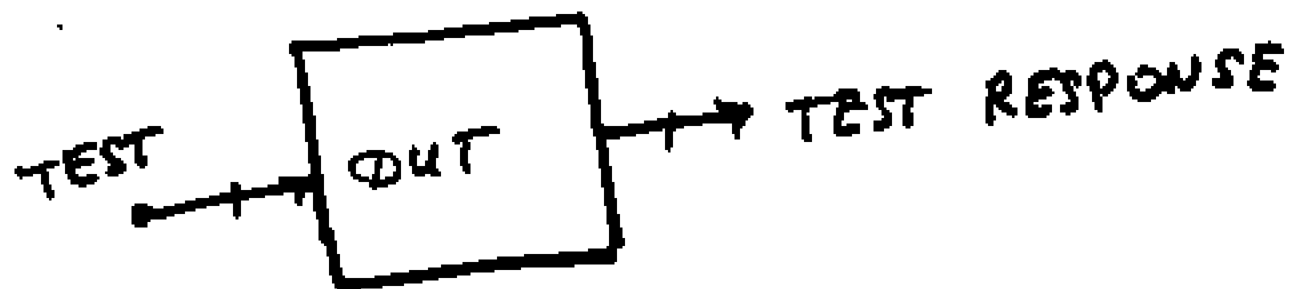
Contributing factors:

∴ High density of gates

∴ Limited number of I/O pins and observation points

∴ Poor controllability and observability of internal lines

∴ LOGICAL DEPTH.



TOPICS:

- TEST GENERATION
- TEST OBSERVATION
- TESTABILITY ANALYSIS
- DESIGN FOR TESTABILITY
- SELF-TESTING
- DIAGNOSTIC

} OFF-LINE TESTING SC752

- FAULT-TOLERANT COMPUTING } ON-LINE SC753

N COMPONENTS IN A DUT

∴ POLYNOMIAL COMPLEXITY ⟹

T(N) – NUMBER OF STEPS IN ATG

$$T(N) \leq \sum_{i=0}^{r} C_i N^i$$

worst case

∴ NP-COMPLETE IFF THERE IS NO ALGORITHM WITH POLYNOMIAL COMPLEXITY

TEST GENERATION IS NP-COMPLETE

APPROACHES TO ATG:

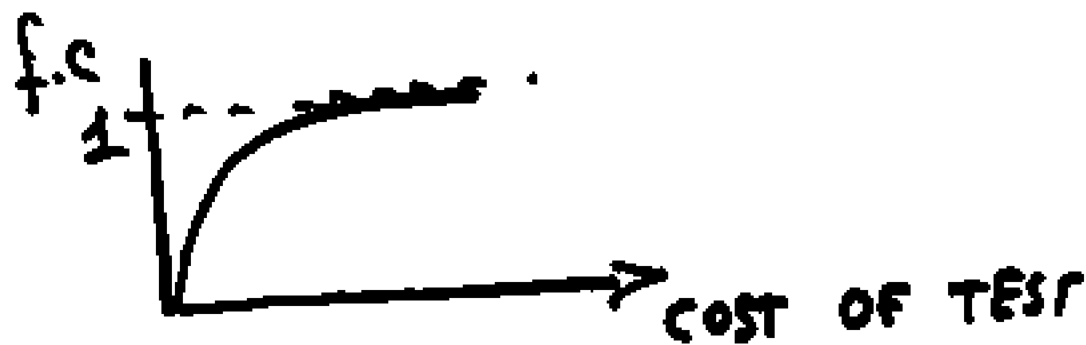
1. DEVELOP NON MINIMAL TESTS (WIDELY USED)

   NUMBER OF TEST PATTERNS

   = C · TEST TIME

2. DETECT LESS THAN 100% OF FAULTS

   f.c. - fault coverage = % of detected faults



3. TEST WHICH ARE EFFICIENT ON AVERAGE

4. TEST FOR EVERY FAULT (NON MINIMAL TEST)
SEPARATELY

5. SELF-ERROR -DETECTION / CORRECTION
ON-LINE TEST