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DESIGN OF SELF-DIAGNOSTIC BOARDS BY SIGNATURE ANALYSIS¹

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Abstract— Two design approaches for self-diagnostic boards based on signature analysis are presented. The goal is to construct a standard chip which can be implemented on any board, such that this chip provides pseudorandom test patterns generation and diagnosis of a faulty chip. This additional chip uses the existing system bus to transfer test data. In the test mode, a sequence of pseudorandom test patterns is applied to all chips on the board-under-test and test responses from chips are compressed into signatures. The first approach is based on testing each chip separately and storing reference signature for every chip. The advantage of this technique is in the multiple-faulty chips diagnostic capability. However, in an operating environment, a single faulty chip is the most likely cause of failure. We present the single-fault-chip diagnostic technique which requires only two reference signatures for any number of chips on the original board. With this technique, one can substantially reduce the hardware overhead compared to the diagnostic technique based on separate testing of each chip on the board. The presented single-faulty-component diagnostic technique can be also used for identification of faulty printed boards in a system or for identification of faulty processors in a multiprocessor system.

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I. INTRODUCTION

We will consider in this paper a design approach for a self-diagnostic board. This approach will not require an external tester for diagnostic and can be used, for example, for manufacturing testing. We note also, that the same approach can be used for identification of a faulty printed board in a computer system or for identification of a faulty processor in a multi-processor system.

An original board consists of several VLSI (LSI) chips without any provision for built-in self test. The transfer of data between chips is implemented via the system bus, (see Fig. 1).

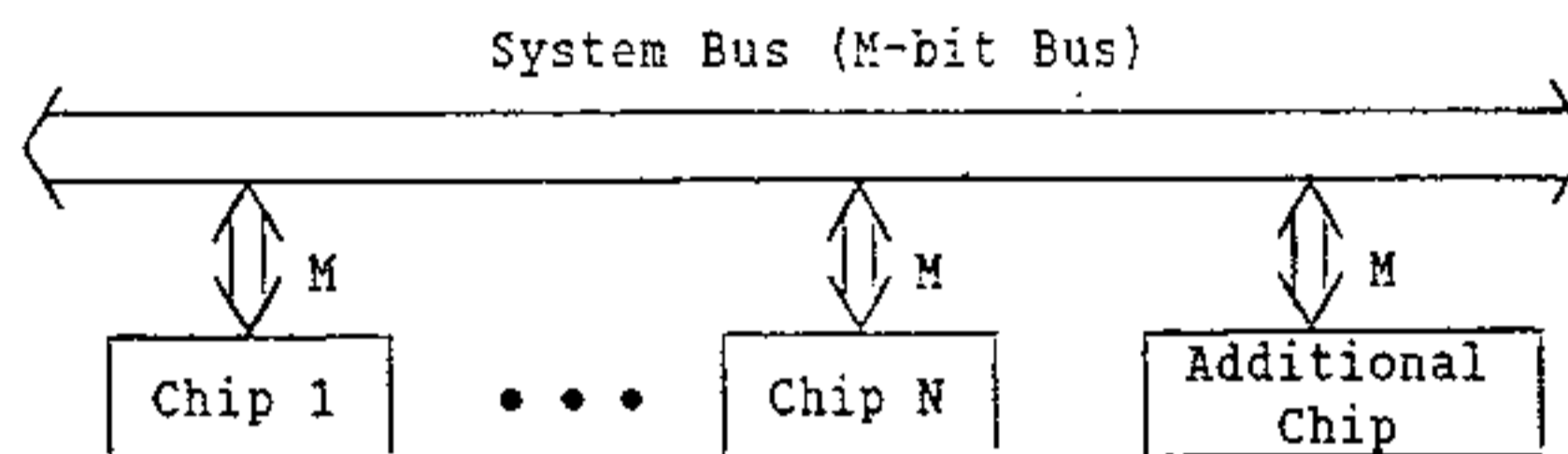


Fig. 1. General Configuration of Self-Diagnostic Board

The goal is to construct an additional chip which provides a self-diagnosis for the original system. The additional chip consists of three components; (i) pseudorandom test patterns generator implemented by a linear feedback shift register (LFSR) [1]-[9], (ii) signature analyzer/diagnosis module and (iii) test/diagnostic procedure controller.

In Section 2, we consider the straightforward approach for self-diagnosis of a board based on separate testing of each chip where all N reference signatures are stored. The hardware complexity for the signature analyzer/diagnosis module of the technique will be given.

The advantage of the straightforward technique is in the multiple-faulty-chip diagnostic capability since each chip is tested separately. However, in

an operating environment, single-faulty-chip events are most likely to occur, hence, a single-faulty-chip diagnostic procedure may be sufficient. In Section 3, we will present a single-faulty-chip diagnostic technique which will require only two reference signatures to be stored for any number of chips, N , on the original board. The hardware complexities for the signature analyzer/diagnosis module are given and compared to the corresponding complexities for the straightforward technique for 16-bit bus systems with $N = 8, 16, 24, 32$ and 64 , chips on the board (see Table 1 and 2). The proposed single-faulty-chip diagnostic approach results in considerable savings in required overhead compared with the straightforward approach.

In Section 4, a brief discussion on estimation of error masking (aliasing) probabilities for signature analysis schemes used in both diagnostic techniques is given.

II. A STRIGHTFORWARD SELF-DIAGNOSTIC DESIGN

For a straightforward self-diagnostic design, each chip is being tested separately and the following cycles of test data transfers are executed. A cycle consists of a generation of a new pseudorandom test pattern which is transferred to the chip being tested, a test response pattern from a chip is then transferred to the parallel-input LFSR, and the LFSR is clocked to its next state. (see Fig. 2, below). The signature of the test responses from the chip is obtained when all T (test length) test patterns are applied. The obtained M -bit signature is then compared with the corresponding reference (bitwise exclusive-OR between the obtained signature and the reference), where any mismatch in the M bits is detected by the output of the M -input OR-gate, (see Fig. 2, below).

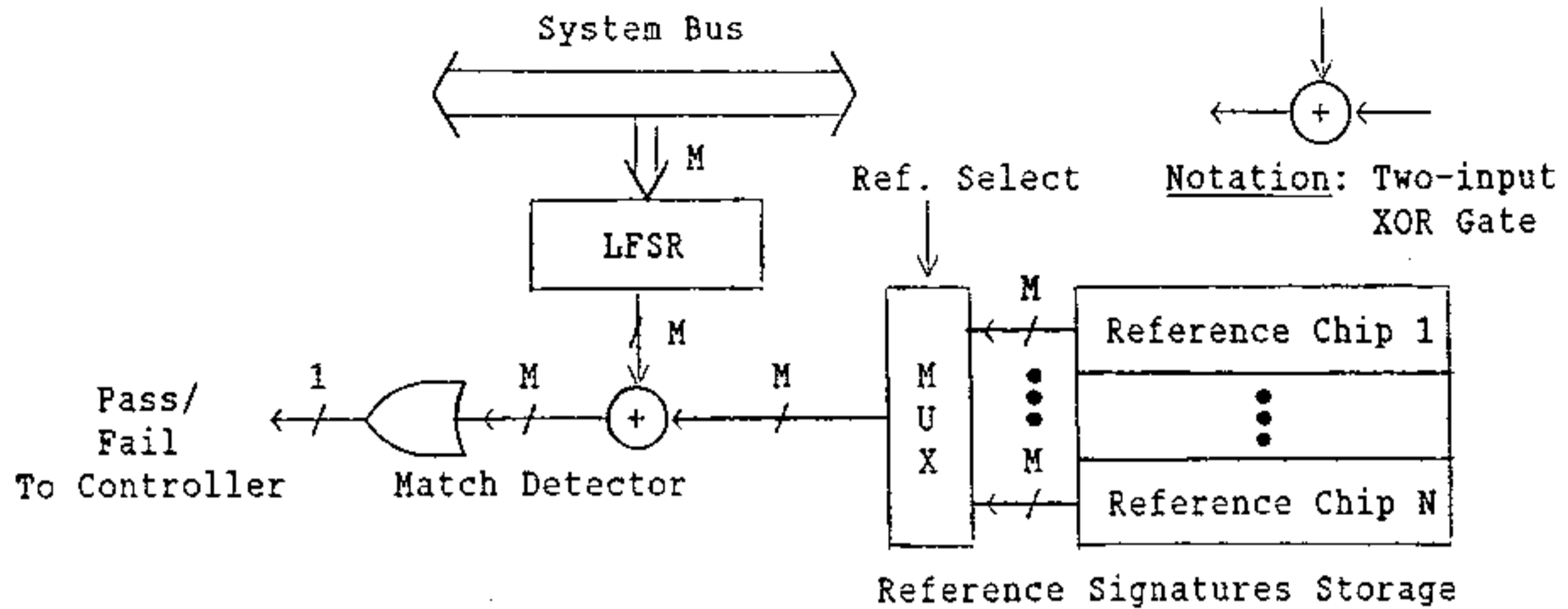


Fig. 2. Straightforward approach—Signature Analyzer/Diagnosis Module

The signature analyzer/diagnosis module for the presented straightforward technique requires: a parallel-input LFSR (see Fig 4, below), a match detector (M two-input exclusive-OR-gates cascaded by an M -input OR-gate), an $N \times 1$ multiplexer, N reference storage registers. The hardware complexity of the straightforward approach measured in terms of equivalent two-input gates (a flip-flop is taken to have the complexity of 12 equivalent two-input gates) is given by

$$L_0(N, M, w) = 13MN + 15M + N[\log_2 N] + w, \quad (1)$$

where N is the number of chips on the board, M , is the width of the system bus and w is the number of internal feedback taps of the LFSR.

III. SINGLE-FAULTY-CHIP SELF-DIAGNOSTIC TECHNIQUE

Since single-faulty-chip events are most likely to occur as a cause of failures in a system, a self-diagnostic procedure capable of locating a single-faulty-chip will be sufficient in many cases. The advantage of the approach presented below over the straightforward approach of Section 2, is that, only two reference signatures are stored for any number of chips on the original board. This results in a considerable decrease in an overhead

required for self-diagnostic compared to the straightforward approach (see formula (9) and Table 2, below).

The test procedure for this technique can be described as follows. Each pseudorandom test pattern is applied to all N chips and test responses are transferred from one chip at a time to the signature analyzer/diagnosis module of the additional chip.

Let $\bar{z}_i(t)$ denote a test response (M -bit vector) from the chip number i , $1 \leq i \leq N$, due to the t th test pattern, $0 \leq t \leq T-1$. Then we have the following string \bar{z} of test responses coming into the signature analysis/diagnosis module:

$$\begin{aligned} \bar{z}: & \bar{z}_N(0), \quad \bar{z}_{N-1}(0), \quad \dots, \quad \bar{z}_j(0), \quad \dots, \quad \bar{z}_1(0), \\ & \bar{z}_N(1), \quad \bar{z}_{N-1}(1), \quad \dots, \quad \bar{z}_j(1), \quad \dots, \quad \bar{z}_1(1), \\ & \dots \\ & \bar{z}_N(t), \quad \bar{z}_{N-1}(t), \quad \dots, \quad \bar{z}_j(t), \quad \dots, \quad \bar{z}_1(t), \\ & \dots \\ & \bar{z}_N(T-1), \quad \bar{z}_{N-1}(T-1), \quad \dots, \quad \bar{z}_j(T-1), \quad \dots, \quad \bar{z}_1(T-1). \end{aligned} \quad (2)$$

The string \bar{z} is represented above as an array of test responses where test responses appear in an t th row are responses from N chips at moment $0 \leq t \leq T-1$ and test responses appear in an i th column are responses from chip number i , $1 \leq i \leq N$, $\bar{z}_i(t)$ for $t = 0, \dots, T-1$. For the situation when only one of the chips is faulty, that is, one of the columns of test responses in (2) contains errors, the problem is to construct a diagnostic procedure to locate the column of test responses that contains errors.

The presented solution in constructing signature analysis scheme is based on space compression techniques [4]-[7] and on nonbinary single-error-correcting Hamming codes [7].

The scheme will require a two-step computation of two M-bit signatures \bar{s} and \bar{s}^* (see Fig. 3).

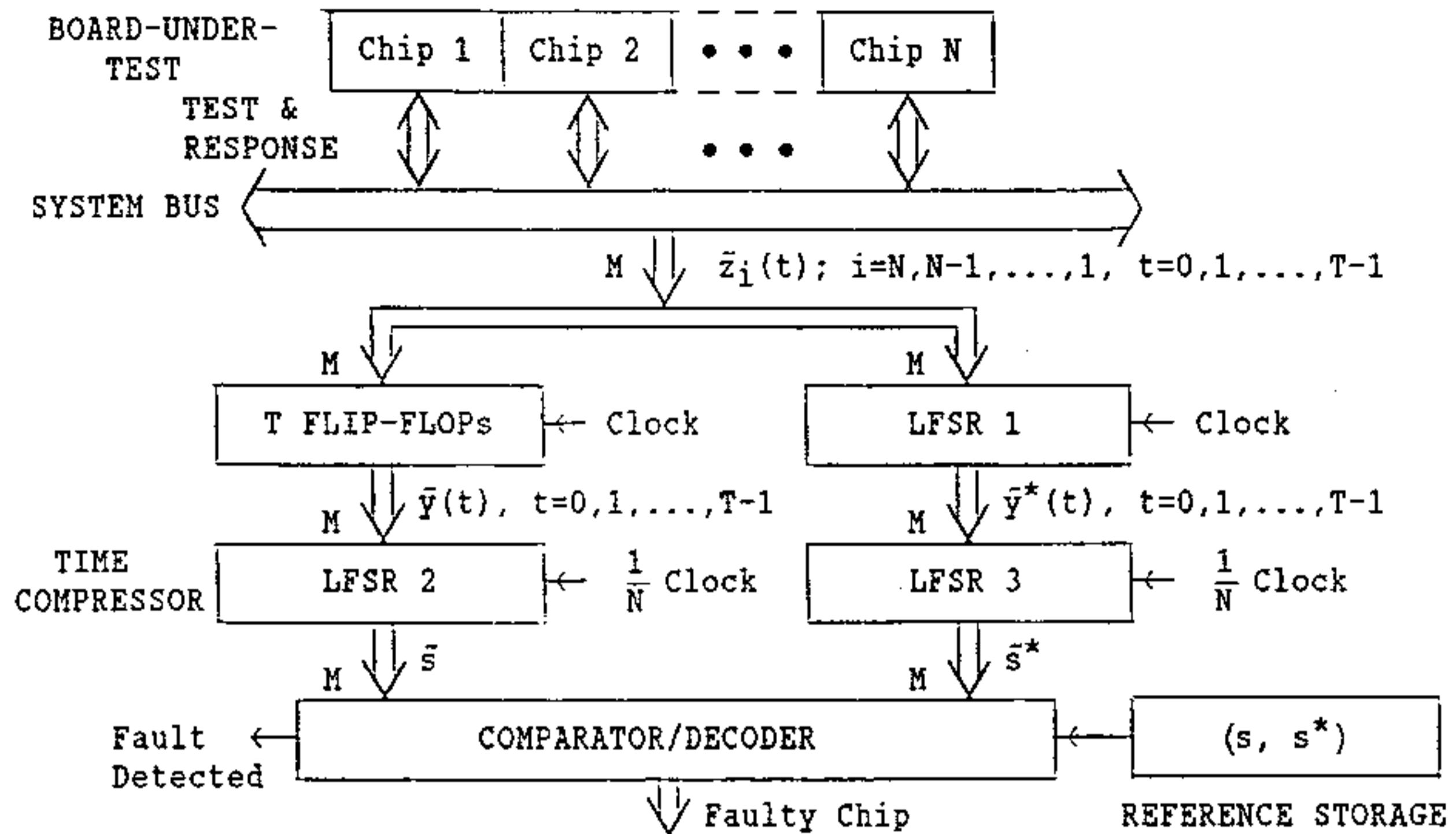


Fig. 3. Single-Faulty-Chip Self-Diagnostic Module

The first step is the computation of two M-bit intermediate signatures $\tilde{y}(t)$ and $\tilde{y}^*(t)$. In Fig. 3, at a moment t , $0 \leq t \leq T-1$, test responses $\tilde{z}_i(t)$, $i = N, N-1, \dots, 1$, are clocked-in the T-Flip-Flop (T-FF) register and LFSR 1 simultaneously, and the contents of the T-FF register and LFSR 1 are $\tilde{y}(t)$ and $\tilde{y}^*(t)$, respectively. (Note, that T-FF register and LFSR 1 have been previously cleared prior to application of $\tilde{z}_i(t)$, $i = N, N-1, \dots, 1$).

We will use algebraic expressions for $\tilde{y}(t)$ and $\tilde{y}^*(t)$ as a tool in explaining how a faulty chip is located. Contents of the T-FF register, $\tilde{y}(t)$, and LFSR 1, $\tilde{y}^*(t)$, after $\tilde{z}_i(t)$, $i = N, N-1, \dots, 1$, $0 \leq t \leq T-1$, are clocked-in are given by

$$\tilde{y}(t) = \tilde{z}_N(t) \oplus \tilde{z}_{N-1}(t) \oplus \dots \oplus \tilde{z}_2(t) \oplus \tilde{z}_1(t), \quad (3)$$

$$\tilde{y}^*(t) = \alpha^{N-1} \tilde{z}_N(t) \oplus \alpha^{N-2} \tilde{z}_{N-1}(t) \oplus \dots \oplus \alpha \tilde{z}_2(t) \oplus \tilde{z}_1(t), \quad (4)$$

where \oplus denotes bitwise exclusive-OR of components of $\bar{z}_i(t)$, α is a primitive element of Galois field of 2^M elements, $GF(2^M)$, (α is a primitive element iff $\alpha^i \neq \alpha^j$ for $i \neq j$, $i, j = 0, 1, \dots, 2^M - 2$), and the products $\alpha^{i-1} z_i(t)$, $i = N, N-1, \dots, 1$, are defined in $GF(2^M)$, [11]-[13]. In (4), α^i and $\bar{z}_i(t)$ are binary M -bit vectors. Multiplications of vectors in (4) are implemented as multiplications of polynomials with binary coefficients modulo some primitive polynomial $p(x)$. A polynomial $p(x) = 1 \oplus q_1x \oplus \dots \oplus q_{M-1}x^{M-1} \oplus x^M$, is primitive if the corresponding autonomous LFSR ($(a_0, \dots, a_{M-1}) = (0, \dots, 0)$, see Fig. 4) runs through all $2^M - 1$ possible nonzero internal states for any nonzero initial state. Tables of primitive polynomials can be found in [6]-[8].

For example, for $M = 4$ and $p(x) = 1 \oplus x \oplus x^4$,

$$(1 \ 1 \ 0 \ 1) \times (1 \ 0 \ 1 \ 0) = (1 \oplus x \oplus x^3)(1 \oplus x) = 1 \oplus x \oplus x^2 \oplus x^5. \quad (6)$$

Since $x^4 \oplus x \oplus 1 = 0$ (modulo $p(x)$), we have $x^5 = x^2 \oplus x$, and substituting this into (5)

$$(1 \ 1 \ 0 \ 1) \times (1 \ 0 \ 1 \ 0) = 1 \oplus x \oplus x^3 \oplus x^2 \oplus x = x \oplus x^2 \oplus x^3 = (0 \ 1 \ 1 \ 1).$$

Expression (4) for $\bar{y}^*(t)$ above describes the state of LFSR 1 after N transitions with inputs $\bar{z}_i(t)$, $i = N, N-1, \dots, 1$. The block diagram of LFSR 1 (primitive LFSR) is given in Fig. 4 where the feedback taps are corresponding to the primitive polynomial over $\{0, 1\}$ of degree M , $p(x) = 1 \oplus q_1x \oplus \dots \oplus q_{M-1}x^{M-1} \oplus x^M$, $q_i \in \{0, 1\}$, [5], [6].

The second step of the signature analysis is the time compression of the intermediate signatures $\bar{y}(t)$ and $\bar{y}^*(t)$, $t = 0, 1, \dots, T-1$, using LFSR 2 and LFSR 3, (see Fig. 3). For each $\bar{y}(t)$ and $\bar{y}^*(t)$ obtained, $\bar{y}(t)$ and $\bar{y}^*(t)$ are clocked-in LFSR 2 and 3, respectively. Next, T-FF register and LFSR 1 are cleared and the process of obtaining $\bar{y}(t+1)$ and $\bar{y}^*(t+1)$ starts. After $\bar{y}(T-1)$

and $\bar{y}^*(T-1)$, are clocked-in LFSR 2 and 3, signatures \bar{s} and \bar{s}^* are obtained.

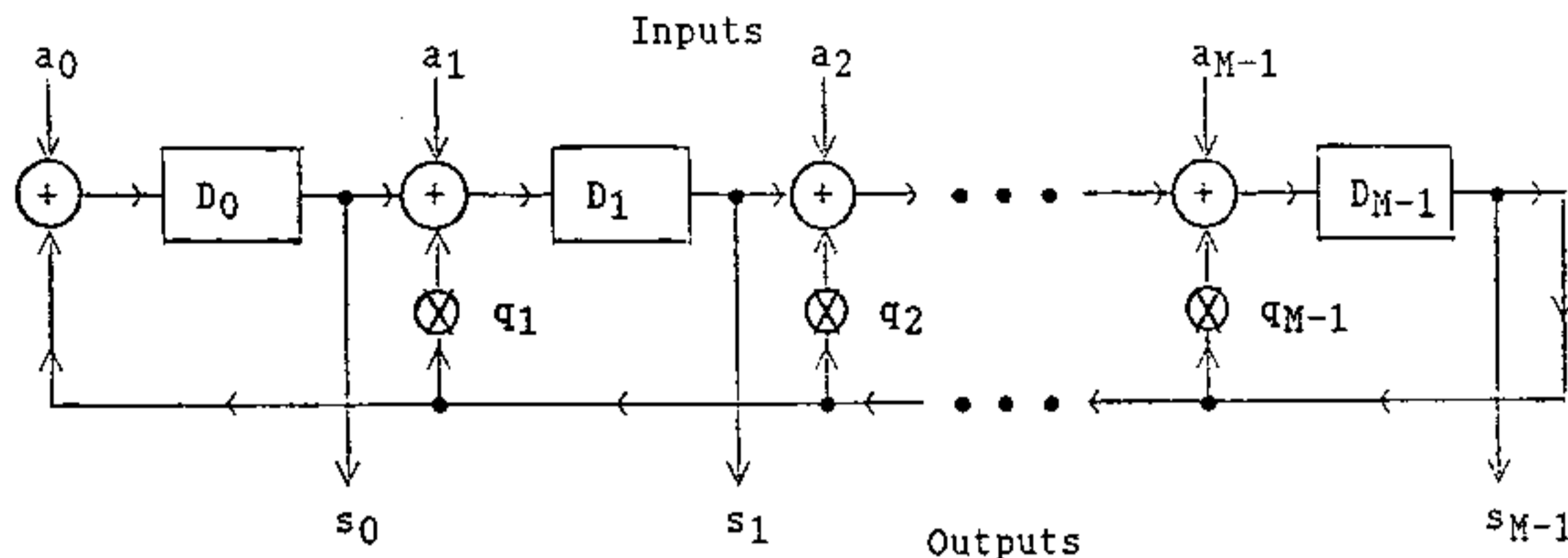


Fig. 4. Block Diagram of Parallel-input LFSR

Looking at the expressions for $\bar{y}(t)$ and $\bar{y}^*(t)$ ((3) and (4)), one can see that $\bar{y}(t)$ is a sum of $\bar{z}_i(t)$, $i = N, N-1, \dots, 1$, and $\bar{y}^*(t)$ is a weighted sum of $\bar{z}_i(t)$ (with the weight α^{i-1} for $\bar{z}_i(t)$). Thus, a distortion in $\bar{z}_j(t)$, $1 \leq j \leq N$, implies that the distortions $\Delta y(t)$ and $\Delta y^*(t)$ in the intermediate signatures $\bar{y}(t)$ and $\bar{y}^*(t)$ are related by $\Delta y^*(t) = \alpha^{j-1} \Delta y(t)$, (where $\Delta y(t) = \bar{y}(t) \oplus y(t)$, and $\Delta y^*(t) = \bar{y}^*(t) \oplus y^*(t)$, are the distortions in $\bar{y}(t)$ and $\bar{y}^*(t)$ with $y(t)$ and $y^*(t)$ being the distortion-free intermediate signatures).

The time compression of the intermediate signatures $\bar{y}(t)$ and $\bar{y}^*(t)$, $t=0, \dots, T-1$ into the final signatures \bar{s} and \bar{s}^* is obtained by LFSR 2 and 3. Since the feedback taps of LFSRs 1, 2, and 3 are the same, the difference equations describing state transitions of these LFSRs are defined over the same finite field $GF(2^M)$ (same modulo polynomials). Thus, we have, for distortions in the signatures \bar{s} and \bar{s}^* , ($\Delta s \triangleq \bar{s} \oplus s$ and $\Delta s^* \triangleq \bar{s}^* \oplus s^*$):

$$\Delta s = \alpha^{j-1} \Delta s^* \quad \text{iff} \quad \{\bar{z}_j(t), t=0, 1, \dots, T-1\},$$

is distorted (chip j is faulty). (7)

The diagnostic procedure is implemented by the comparator/decoder (see Fig. 3). The outputs of the comparator (see Fig. 5, below), Δs and Δs^* , are

componentwise exclusive-OR between obtained signature \bar{s} , \bar{s}^* and the reference s , s^* . If $(\Delta s, \Delta s^*) = (0, 0)$, we conclude that the system is fault-free.

If $(\Delta s, \Delta s^*) \neq 0$, the diagnostic procedure described in (7) is implemented by a decoder. In Fig. 5, the autonomous LFSR generates the products $\alpha^{i-1}\Delta s$, $i=1, 2, \dots, N$, with its initial state of the LFSR being Δs . This autonomous LFSR is characterized by

$$s(k+1) = \alpha s(k), \quad s(0) = \Delta s, \quad 0 \leq k \leq N-1, \quad (8)$$

and after the k th shift the content of the LFSR is equal to $\alpha^k \Delta s$.

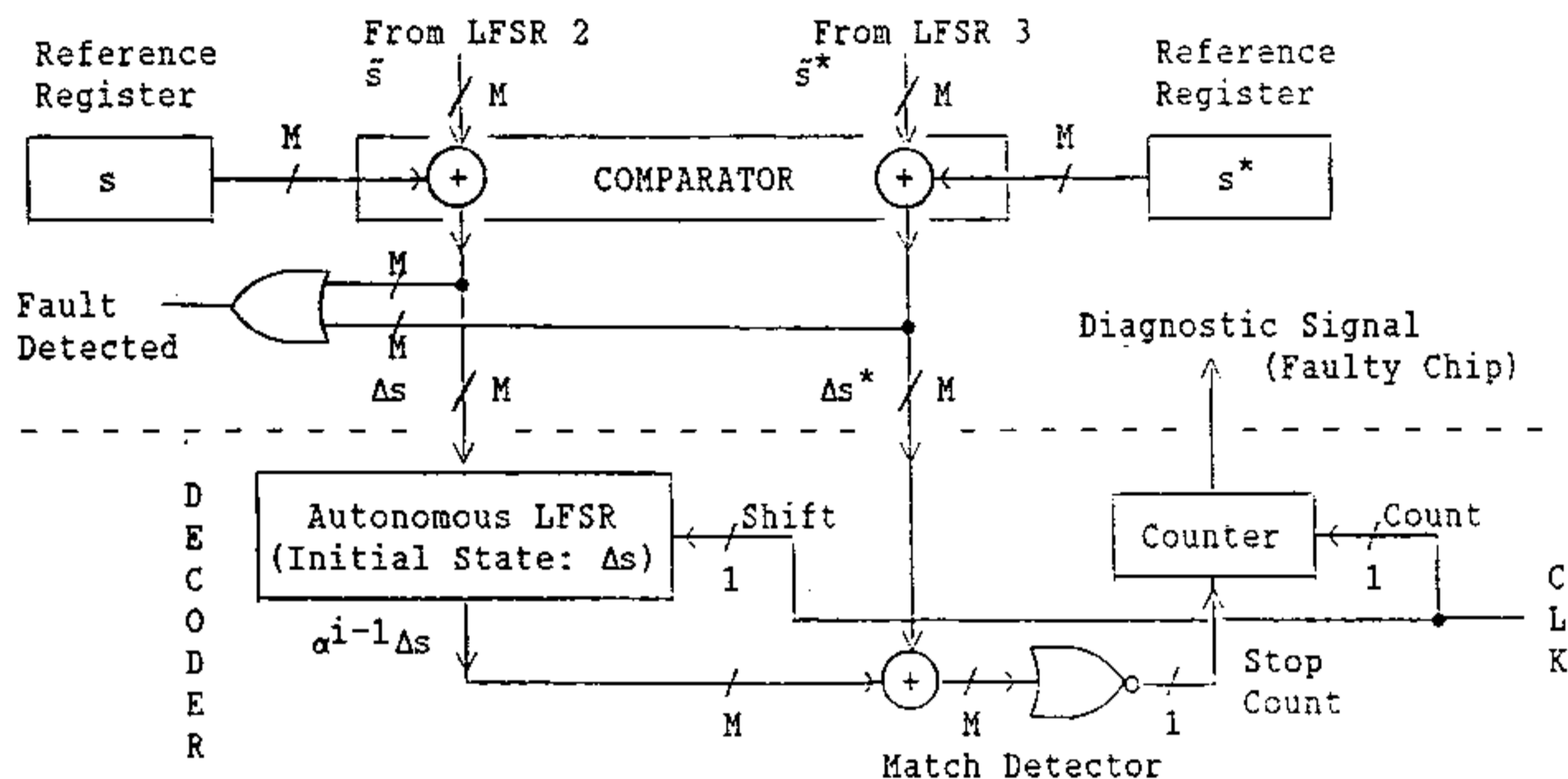


Fig. 5. Comparator and Decoder

The function of the decoder shown in Fig. 5 can be described as follows. First, Δs is loaded into the autonomous LFSR and its content is componentwise exclusive-ORed with Δs^* . (The shift in the autonomous LFSR and the count of the counter are controlled by the same clock signal). If $\alpha^{j-1}\Delta s = \Delta s^*$ for some j ($1 \leq j \leq N$), then the "stop count" signal is equal to one (indicating a match between $\alpha^{j-1}\Delta s$ and Δs^*), the counting stops and the

counter's internal state indicates a faulty chip j .

In comparing the hardware complexities of the additional chips for the straightforward approach and the single-faulty-chip diagnostic approach, we will focus on the complexities of the signature analyzer/diagnosis modules leaving out the complexities of the test generation and control modules. (Note that, the control and test generation modules for both approaches have approximately the same order of complexities).

The presented single-faulty-chip diagnostic approach requires: four M -bit parallel-input LFSRs, one M -bit T-FF register, two M -bit registers storing references s and s^* and a counter modulo N . The total hardware overhead for the redundant chip is given by,

$$L_1(M, N, w) = 104M + 4w + 2 + 12 \lceil \log_2 N \rceil, \quad (9)$$

equivalent two-input gates.

In Table 1, we show a comparison of the hardware complexities between the straightforward approach and the single-faulty-chip diagnostic approach for the case of 16-bit bus system ($M = 16$) and for the number of chips on the board $N = 8, 16, 24, 32$ and 64 . Since the number N of reference signatures required for the single-faulty-chip approach is always two, the advantage of this approach over the straightforward approach is more apparent with an increasing N . Table 2 shows savings P in gate counts we gain when using the proposed single-faulty-chip diagnostic approach.

Approach	N				
	8	16	24	32	64
Straightforward	1,931	3,579	5,355	7,059	13,939
Single-Faulty-Chip Diagnostic	1,714	1,726	1,738	1,738	1,762

Equivalent two-input gate counts

Table 1. Overheads for Different Numbers of Chips N on the Board for 16-Bit System Bus.

N	8	16	24	32	64
P	11%	52%	68%	75%	87%

Table 2. Percentages-Savings P in Overheads of Single-Faulty-Chip Diagnostic Over Straightforward Approach For 16-Bit System Bus.

IV. EXAMPLE

Let us consider the board-under-test with $N = 5$ chips and $M = 3$ outputs per chip. Since the proposed signature analysis scheme consists of two cascaded linear mappings (intermediate signatures $\tilde{y}(t)$ and $\tilde{y}^*(t)$ followed by the time compression of $\{\tilde{y}(t), t=0, \dots, T-1\}$ and $\{\tilde{y}^*(t), t=0, \dots, T-1\}$ using two separate LFSRs), for the observed test responses $\tilde{z} = z \oplus e$, written as the componentwise exclusive-OR of the fault-free responses and errors, the signatures of \tilde{z} , \tilde{s} , \tilde{s}^* are equal to the componentwise exclusive-OR of the signatures of z and e , that is, $\tilde{s} = s \oplus \Delta s$ and $\tilde{s}^* = s^* \oplus \Delta s^*$. Hence, an example showing how the proposed signature scheme locates a faulty chip can be presented in terms of the analysis of the signatures of errors Δs and Δs^* .

be

Let the feedback polynomial of the LFSRs equal to $p(x) = x^3 \oplus x \oplus 1$. Then, nonzero elements of $GF(2^3)$ ($M = 3$) are given in Table 3 which also are the outputs (internal states) of the autonomous LFSR with this feedback polynomial (see Fig. 6) and initial state equal to $(1\ 0\ 0) = 1$. The vector representation of an element of $GF(2^3)$ corresponds to the coefficients of $s_0 \oplus s_1x \oplus s_2x^2$ and the exponential representation for the nonzero elements of $GF(2^3)$ is given as the power of a primitive element α chosen as $\alpha = (0\ 1\ 0) = x$ such that $\{\alpha^i, i=0, \dots, 6\}$ is the set of all nonzero elements in $GF(2^3)$, moreover, $\alpha^i \alpha^j = \alpha^{(i+j) \bmod 7}$.

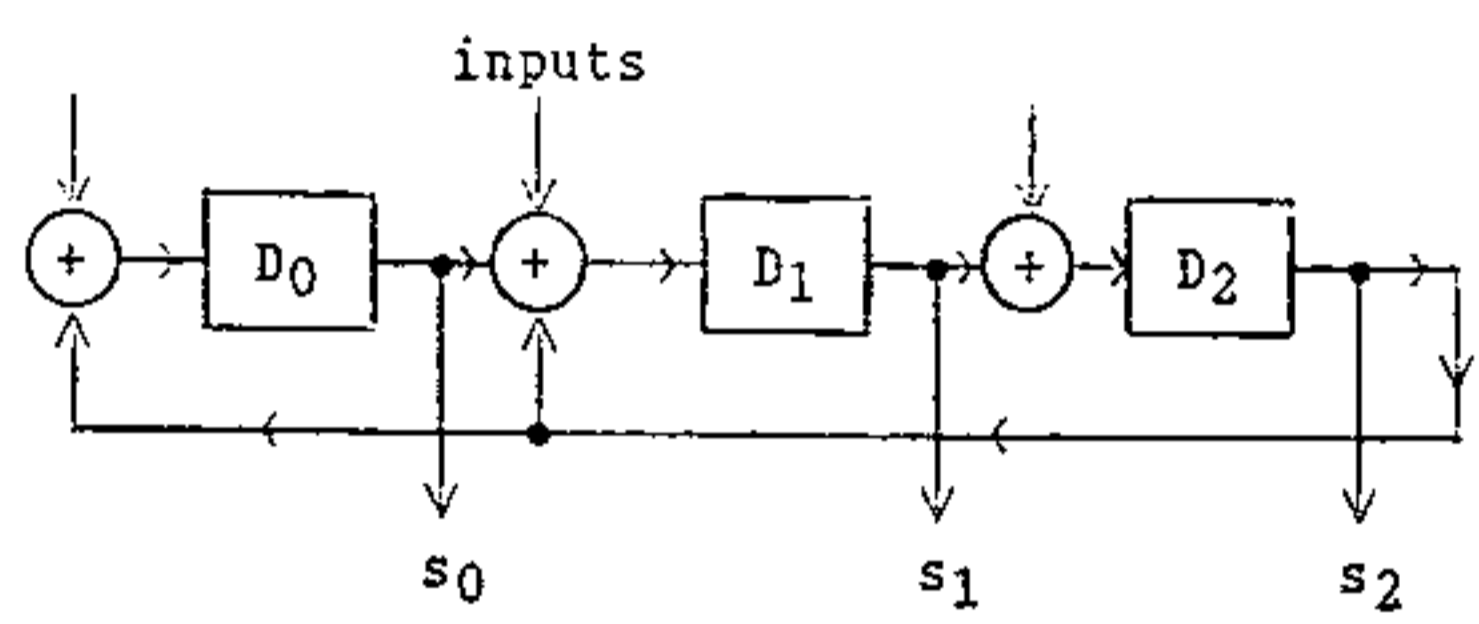


Fig. 6. Block Diagram of LFSRs— Example

t	inputs	s ₀	s ₁	s ₂	α^t
0	0 0 0	1	0	0	1
1	0 0 0	0	1	0	α
2	0 0 0	0	0	1	α^2
3	0 0 0	1	1	0	α^3
4	0 0 0	0	1	1	α^4
5	0 0 0	1	1	1	α^5
6	0 0 0	1	0	1	α^6
7	0 0 0	1	0	0	1

Table 3. Nonzero Elements of $GF(2^3)$ with $p(x) = x^3 \oplus x \oplus 1$

An example of the analysis of distortion in signatures, A_s and A_s^* , illustrating the diagnostic rule: $A_s = \alpha^{j-1} A_s^*$ iff chip j is faulty, $1 \leq j \leq N$, is presented below.

Let us consider errors in the test responses presented as an $(e_i(t))$ array of elements in $GF(2^3)$ where the entries in the t th row are errors in the test responses at moment $0 \leq t \leq 5$, and the entries in the i th column are errors produced by the chip i , $1 \leq i \leq 5$:

$$(e_i(t)) = \begin{matrix} & \begin{matrix} \underline{5} & \underline{4} & \underline{3} & \underline{2} & \underline{1} \end{matrix} \\ \begin{matrix} \left(e_i(t) \right) \end{matrix} & = & \begin{pmatrix} 0, & \alpha^6, & 0, & 0, & 0, \\ 0, & 0, & 0, & 0, & 0, \\ 0, & 0, & 0, & 0, & 0, \\ 0, & \alpha, & 0, & 0, & 0, \\ 0, & \alpha^5, & 0, & 0, & 0, \\ 0, & 1, & 0, & 0, & 0. \end{pmatrix} \end{matrix} \quad (10)$$

In this case we have the chip number four being faulty with the error $e_4(t) = (\alpha^6, 0, 0, \alpha, \alpha^5, 1)$ and errors are zeros for other chips ($e_i(t) = 0$, for all t , $i = 0, 1, 2, 3, 5$). The intermediate signatures of errors at a moment $0 \leq t \leq 5$ are given by $\Delta y(t) = e_5(t) \oplus e_4(t) \oplus \dots \oplus e_1(t)$ and $\Delta y^*(t) = \alpha^4 e_5(t) \oplus \alpha^3 e_4(t) \oplus \dots \oplus e_1(t)$. The intermediate signatures of errors $\Delta y(t)$ (obtained by the T-flip-flop register) and $\Delta y^*(t)$ (obtained by LFSR 1) ^{are} shown in Table 5. We will now show as an example the state transitions of LFSR 1 in obtaining the intermediate signature of errors at moment $t = 0$, $\Delta y^*(0) = \alpha^3 e_4(0) = \alpha^3 \alpha^6 = \alpha^{9 \bmod 7} = \alpha^2 = (0 \ 0 \ 1)$, in the following table.

Shift i	$e_{5-i}(0)$	State of LFSR 1		
		s_0	s_1	s_2
0	$(0 \ 0 \ 0) = 0$	0	0	0 (initial value)
1	$(1 \ 0 \ 1) = \alpha^6$	0	0	0
2	$(0 \ 0 \ 0) = 0$	1	0	1
3	$(0 \ 0 \ 0) = 0$	1	0	0
4	$(0 \ 0 \ 0) = 0$	0	1	0
5	don't care	0	0	1 = $\Delta y^*(0)$

Table 4. State transition of LFSR 1 in obtaining $\Delta y^*(0)$

In Table 5 (below), we show the state transitions of LFSR 2 and 3, with

inputs being the intermediate signatures of errors $\Delta y(t) = e_4(t)$ and $\Delta y^*(t) = \alpha^3 e_4(t)$, $t=0, \dots, 5$. The distortions in signatures satisfy $\Delta s^* = \alpha^6 = \alpha^3 \Delta s$, since chip number four is faulty.

t	Inputs of LFSR 2 $\Delta y(t)$	State of LFSR 2 $s_0 s_1 s_2$	Inputs of LFSR 3 $\Delta y^*(t)$	State of LFSR 3 $s_0 s_1 s_2$
0	$\alpha^6 = (1 0 1)$	0 0 0	$\alpha^3 \alpha^6 = (0 0 1)$	0 0 0
1	0 0 0	1 0 1	0 0 0	0 0 1
2	0 0 0	1 0 0	0 0 0	1 1 0
3	$\alpha = (0 1 0)$	0 1 0	$\alpha^3 \alpha = (0 1 1)$	0 1 1
4	$\alpha^4 = (0 1 1)$	0 1 1	$\alpha^3 \alpha^4 = (1 0 0)$	1 0 0
5	1 = (1 0 0)	1 0 0	$\alpha^3 = (1 1 0)$	1 1 0
6	don't care	$\Delta s = (1 1 0)$	don't care	$\Delta s^* = (1 0 1)$

Table 5. State transitions of LFSR 2 and 3

The decoding of the relation between the obtained Δs and Δs^* , $\Delta s^* = \alpha^{j-1} \Delta s$ iff chip j is faulty, $1 \leq j \leq 5$, is done by obtaining $\alpha^{j-1} \Delta s$ which is compared with Δs^* . The product $\alpha^k \Delta s$, $0 \leq k \leq 4$, is the content of the autonomous LFSR with initial state $\Delta s = (1 1 0)$ after k shifts. In Table 6, we show the contents of the autonomous LFSR (see Fig. 6) with initial state $\Delta s = (1 1 0) = \alpha^3$, where the content of the LFSR is $\alpha^k \alpha^3$ after k shifts.

Shift $k = j-1$	State of the Autonomous LFSR $s_0 s_1 s_2$
0	$(1 1 0) = \alpha^3 = \Delta s$
1	$(0 1 1) = \alpha^4$
2	$(1 1 1) = \alpha^5$
3	$(1 0 1) = \alpha^6 = \Delta s^*$ implies chip 4 is faulty
4	$(1 0 0) = \alpha^7 = 1$

Table 6. State transition of the Autonomous LFSR of the Decoder

For $k = 3$ one can see that $\Delta s^* = \alpha^6 = \alpha^3 \Delta s = \alpha^3 \alpha^3$, this indicates that chip number $j = k+1 = 4$ is faulty.

V. THE ERROR-MASKING PROBABILITIES

With the single-faulty-chip model distorted test responses from a faulty chip can result in \bar{s} and \bar{s}^* which are equal to the reference signatures. This situation is known as 'error-masking event' which means a miss-detection of a faulty chip by the signature analysis. It is important to point out that an estimation of an error-masking (aliasing) probability, [8], [9], must be based upon an M-bit signature scheme, since \bar{s}^* is a multiple of \bar{s} , ($\Delta s^* = 0$ iff $\Delta s = 0$). For the assumption that errors (manifestation of faults) are equiprobable, both approaches attain the error-masking probabilities equal to 2^{-M} . Moreover, for the number of faulty chips $L > 1$, the straightforward approach attains the error-masking probability 2^{-LM} and the single-faulty-chip diagnostic approach attains the error-masking probability of 2^{-2M} . However, we must keep in mind that 2^{-M} is often sufficient (typically $M = 16$ or 32), moreover, single-faulty-chip occurrences are the most probable types of system failures.

VI. CONCLUSIONS

The proposed method for a design of self-diagnostic board under single-faulty-chip assumption is based on a standard additional chip which can be implemented on any board and uses an existing system bus for transferring test data. The structure of this redundant chip depends only on two parameters, M number of output lines per chip and N number of chips on a board. This method does not require a board to have built-in self-testing chips.

The proposed approach is based on the signature analysis and requires only two reference signatures for any number of chips on the original board. Hence, with this approach one substantially reduces the hardware overhead in

a design of a self-diagnostic system. For example, for a self-diagnostic board with 32 chips and 16-bit system bus, by the proposed approach one saves 75% of the hardware overhead compared with the straightforward approach when each one of the chips on the board is tested separately by a linear feedback shift register. We note, that the proposed method can be also used for identification of faulty printed boards in a system or for identification of faulty processors in a multiprocessor system.

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