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BOARD-LEVEL DIAGNOSIS BY SIGNATURE ANALYSIS*

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Abstract

Board-level diagnostic techniques by signature analysis based on single-error-correcting Hamming codes over $GF(2^M)$ (where M is the number of outputs per chip) are presented. We consider two techniques; (i) the space-time compressor technique for the case when responses from N chips on the board are wired to the compressor and (ii) the time compressor technique for the case when test responses from each chip are transferred to the compressor via system bus. Assuming a single-faulty-chip model, a faulty chip on the board-under-test is located by an analysis of the relationship between the distortions in the obtained signatures. Both techniques for board-level diagnosis require less hardware than the straightforward diagnostic techniques using (i) built-in signature analyzer for every chip or (ii) selectively testing of each chip via system bus, hence offer an efficient approach for a design of a built-in-self-test board and for manufacturing testing.

1 Introduction

We will consider in this paper the problem of board-level diagnostic which is one of the most difficult problems in testing. We assume that the original board consists of several VLSI (LSI) chips without any provision for built-in-self-test (BIST). The proposed design of BIST board will require additional redundant chips. In the test mode, these chips automatically (i) generate test patterns (for example pseudorandom vectors by an LFSR), (ii) compress test responses into a signature, (iii) compare the signature with the reference and (iv) locate a faulty-chip(s) when faults are detected.

The terms parallel diagnosis and serial diagnosis will be used for the approaches where test appication and compression of responses are performed simultaneously for all chips on the board-under-test and each chip is tested one at a time with resoponses are serially transferred via system bus to the compressor respectively. Note that, in order to diagnose (locate) faulty chips, we disconect all chips in the testing mode, to confine manifestations of faults (errors) within the outputs of the chips on the board-under-test.

The advantage of parallel diagnosis over serial diagnosis lies in the test time. Since for board-under-test consisting of N chips, the time required to apply and observe T test patterns and responses via system bus for the case of serial diagnosis is proportional to NT. In comparison, parallel diagnosis, (parallel application of test patterns to all N chips), requires a test time proportional to T. Obviously, the disadvantange of parallel diagnosis is in the hardware overhead.

Two straightforward approarches in achieving a diagnostic capability for the parallel and serial dianosses by signature analysis are (i) provide for every chip parallel application of test patterns and separate signature analyzers and (ii) test individual chips one at a time via system bus using one signature analyzer.

The straightforward approaches have their major draw back in the hardware overhead since these appoarches require N registers storing the fault-free signatures of N chips. Another disadvantage is related to the necessity of precomputing signatures (which may be time consuming). The advantage of the straightforward approaches is the diagnostic capability with respect to multiple faulty chips. However, the multiple-faulty-chips diagnostic testing may not necessarily be the goal if the probabilities that any chip being faulty are independent so that the single-faulty-chip events are the most probable. In the following sections we describe two diagnostic techniques based on the single-faulty-chip model, with the intention that, these techniques will require less hardware overhead.

Two single-faulty-chip diagnostic techniques we present below (Section 2 and 3) result in a decrease the required hardware overhead. As will be seen, the proposed board-level diagnosis by signature analysis will require two fault-free signatures to be stored (in comparison to N fault-free signatures for the straightforward approaches) and furthermore, for the case of parallel diagnosis three LFSRs are used (in comparison to N LFSRs of the straightforward approach).

*This work was supported by the National Science Foundation under Grant DCR-8317763.

Both approaches can be useful not only for BIST environment but also for diagnosis during a manufacturing testing. For example, a batch of chips can be tested simultaneously by means of a tester board.

2 Parallel Board-Level Diagnosis by Signature Analysis Based on Space-Time Compression of Test Responses

The proposed diagnostic technique is the continuation of our research studies on space compressors [1-3]. (Several techniques for compression of test responses may also be found in [4-7]). It is well-known that space compressors which are decoders of single-error-correcting codes have a diagnostic capability. However, techniques for locating a faulty chip by the signature analysis (compression of a sequence of test responses in time) have not been investigated in depth. (We note also that the diagnostic capability of the signature analysis at the gate-level is very limited [8]).

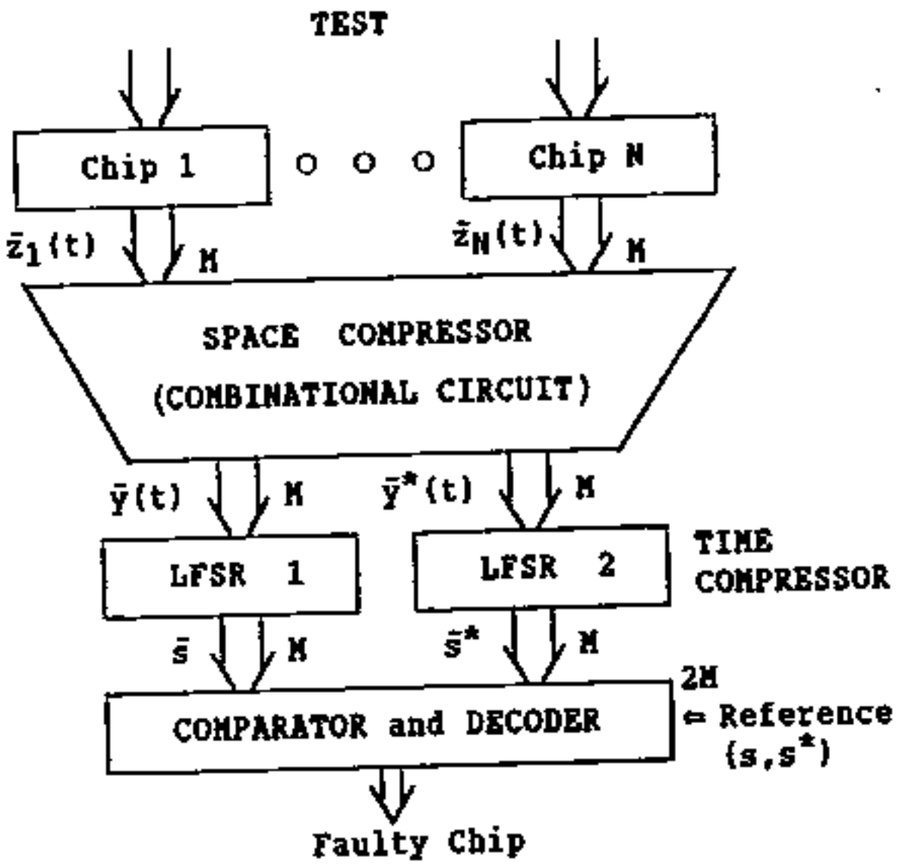

Fig. 1. Parallel Board-Level-Diagnosis by Signature Analysis

In this section we will describe a solution of the parallel board-level diagnostic problem based on a space-time compression technique (see Fig. 1) such that the single-faulty-chip diagnostic capability of the space compressor is preserved under the time compression of the outputs of the space compressor. We note that the parallel diagnosis is obtained by a parallel wiring from the board-under-test's outputs to the space compressor as shown in Fig. 1.

For simplicity, we assume that every chip has the same number of outputs equal to M (see Fig. 1). (Furthermore, for the case of unequal number of outputs per chip we let M be equal to the maximum number of outputs for a chip on the board and assign additional zero components to the outputs of chips with less than M output lines). Let $\bar{z}(t) = (\bar{z}_1(t), \bar{z}_2(t), \ldots, \bar{z}_N(t))$ be a response of the board-under-test at the moment t, $0 \le t \le T-1$, (T is a number of test patterns applied). A component of $\bar{z}(t)$ (board response at moment t), $\bar{z}_i$, $1 \le i \le N$, is an M-bit symbol corresponding to the output of the chip No i. Further, we assume that only one chip may be faulty, that is, at most one component of $\bar{z}$ may be distorted. The space compressor, will be a decoder for a nonbinary (M bit per symbol) single-error-correcting code, and it is capable of locating the distorted $\bar{z}_i$. Since $\bar{z}_i$ is an M-bit symbol, it is convenient to consider the codes which are defined over a finite field of 2^M elements, $GF(2^M)$. We will consider Hamming codes over $GF(2^M)$ where codewords $v = (v_1, v_2, \ldots, v_N)$ are vectors in an N-dimensional space, v_N, over $GF(2^M)$, $v_i \in GF(2^M)$.

2.1 Board Diagnosis by Hamming Codes over $GF(2^M)$—The Space Compressor

A code C is a single-error-correcting linear (Hamming) code if every codeword v has the number of nonzero components (Hamming weight) greater than or equal to three. Single-error-correcting code C over $GF(2^M)$ with block size N and the number of redundant symbols equal to two can be defined by the check matrix H as follows

$$C = \{v \mid vH^T = 0\},$$

$$H = \begin{pmatrix} 1 & 1 & 1 & 1 & \cdots & 1 \\ 1 & \alpha & \alpha^2 & \alpha^3 & \cdots & \alpha^{N-1} \end{pmatrix}, \qquad (1)$$

where $N \le 2^M-1$, H^T denotes transpose of H, and α is a primitive in $GF(2^M)$, that is $\alpha^i \ne \alpha^j$ $(i \ne j, i,j = 0,1,\ldots,2^M-2$ [9,10].

Consider a board response at moment t, $\bar{z}(t) = (z_1(t), \bar{z}_2(t), \ldots, \bar{z}_N(t))$. Then $\bar{z}(t)$ can be expressed as a componentwise modulo two sum of the fault-free response $z(t) = (z_1(t), z_2(t), \ldots, z_N(t))$ and error $e(t) = (e_1(t), e_2(t), \ldots, e_N(t))$,

$$(\bar{z}_1(t), \ldots, \bar{z}_N(t)) = (z_1(t), \ldots, z_N(t)) \oplus (e_1(t), \ldots, e_N(t)) \qquad (2)$$

where $\bar{z}_i(t) \in GF(2^M)$, M is the number of outputs per chip. Consider the case when e(t) is nonzero. If $\bar{z}(t)$ is an input to the compressor, the output of the space compressor is given by $\bar{z}(t)H^T = (z(t) \oplus e(t))H^T$, H is defined by (1). Then, we have:

$$e(t)H^T = \bar{z}(t)H^T \oplus z(t)H^T \triangleq (\Delta y(t), \Delta y^*(t)),$$

$$\Delta y(t), \Delta y^*(t) \in GF(2^M), \qquad (3)$$

and

chip No i is faulty iff $\Delta y^*(t) = \alpha^{i-1}\Delta y(t)$, $1 \le i \le N$.

2.2 Time Compression for Outputs of Space Compressor

The board-level diagnosis by signature analysis is based on a space-time compression technique. At every moment t, t=0,1,...,T-1, the output of the board-under-test $\tilde{z}(t) = (\tilde{z}_1(t),\tilde{z}_2(t),\ldots,\tilde{z}_N(t))$ is first compressed by the space compressor which is a combinational circuit (see Fig. 1).

Let us consider the time compression of the sequences $\{\tilde{y}(t)\}$ and $\{\tilde{y}^*(t)\}$, t=0,1,...,T-1, which are the outputs of the space compressor when a sequence of T test patterns is applied. The sequences $\{\tilde{y}(t)\}$ and $\{\tilde{y}^*(t)\}$ are compressed in time by two separate parallel-input LFSRs. These LFSRs are characterized by

$$\tilde{s}(t+1) = \alpha\tilde{s}(t)\circledast\tilde{y}(t+1) \text{ and } \tilde{s}^*(t+1) = \alpha\tilde{s}^*(t)\circledast\tilde{y}(t+1),$$

$$\tilde{s}(0) = \tilde{s}^*(0) = 0,\ t=0,\ldots,T-1. \qquad (4)$$

The above linear recurrences are defined over $GF(2^M)$ where $\alpha \in GF(2^M)$ is a primitive element of $GF(2^M)$; $\tilde{s}(t)$ and $\tilde{s}^*(t)$ denote the internal states of the two LFSRs at the moment t. (The realization of (4) by parallel-input LFSRs will be discussed in Section 2.3).

Let $\bar{s}=\tilde{s}(T)$ and $\bar{s}^*=\tilde{s}^*(T)$ (see (4)) denote the time signatures for the sequences $\{\tilde{y}(t)\}$ and $\{\tilde{y}^*(t)\}$, t=0,1,...,T-1, respectively, and let Δs and Δs^* be the distortions in $\bar{s}$ and $\bar{s}^*$ obtained by the componentwise exclusive OR sum of $\bar{s}$ and $\tilde{s}^*$ and the reference s and s^*. One can see from (3) and (4) that,

$\Delta s^* = \alpha^{i-1}\Delta s$ $(\Delta s^* \neq 0, \Delta s \neq 0)$, iff

chip No i is faulty. (5)

2.3 Hardware Implementation of The Time Compressor

Fig. 2 shows a block diagram for the parallel-input LFSR implementing (4). Further, it is necessary that the feedback polynomial of the LFSR, $p(x) = x^M \circledast q_{M-1}x^{M-1} \circledast q_{m-2}x^{M-2} \circledast \ldots \circledast 1$, $q_i \in \{0,1\}$, is the same primitive polynomial as the one in the construction of $GF(2^M)$ in (1) (see Example 1, below).

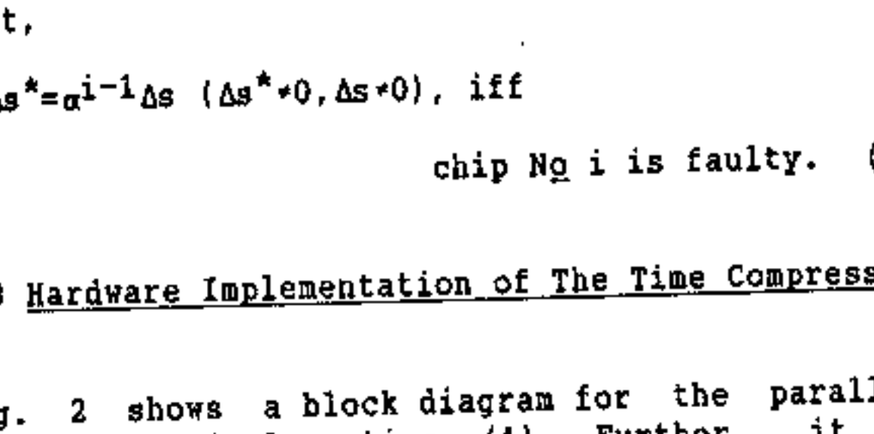

Fig. 2. Block Diagram of Parallel-input LFSR—The Time Compressor

2.4 Diagnostic Procedure for The Space-Time Signature Analysis

We now summarize the parallel diagnostic testing approarch for a board with single-faulty-chip model based on space-time compresion (see Fig. 1). From the top of Fig. 1 a time sequence of T test patterns is applied. For every test pattern the board response is a block of N M-bit symbols (responses from N chips-under-test). A board response at every momemt t, $0 \leq t \leq T-1$ is compressed in space into two M-bit symbols which are separately fed into two LFSRs. The LFSRs are then clocked to a next state completing the compression (space-time) for the applied t th test pattern.

After all T test patterns have been applied, the final internal states of the two LFSRs (signature of the board-under-test) $\bar{s} = \tilde{s}(T)$ and $\bar{s}^* = \tilde{s}^*(T)$ (see (4)) are compared to the reference (s,s^*). The result of the comparison (componentwise exclusive OR) between obtained signature $(\bar{s},\bar{s}^*)$ and the reference is denoted by $(\Delta s,\Delta s^*)$. If $(\Delta s,\Delta s^*) = (0,0)$, we conclude that the system is fault-free.

If $(\Delta s,\Delta s^*) \neq (0,0)$, the diagnostic procedure decribed in (5) is implemented by a decoder. Fig. 3 shows a block diagram of the decoder which generates the products $\alpha^{i-1}\Delta s$, i=1,2,...,N, by an autonomous LFSR with its initial state being Δs. This autonomous LFSR is characterized by the following linear recurrence over $GF(2^M)$,

$$s(j+1) = \alpha s(j),\ s(0)=\Delta s,\ 0 \leq j \leq N-1, \qquad (6)$$

and hence after the j th shift the content of the LFSR is equal to $\alpha^j\Delta s$.

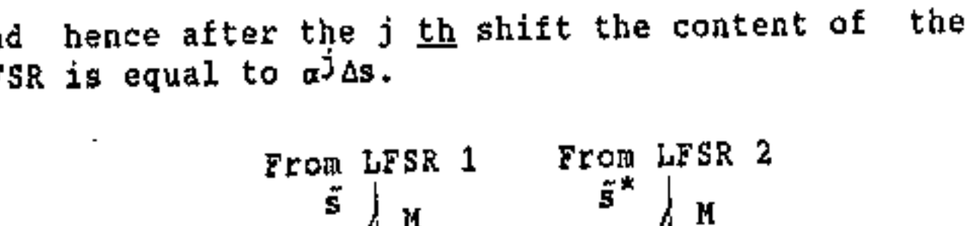

Fig. 3. Comparator and Decoder

The function of the comparator and decoder shown in Fig.3 can be described as follows. The comparator generating $(\Delta s,\Delta s^*)=(\bar{s}\circledast s,\bar{s}^*\circledast s^*)$ is implemented by two componentwise exclusive ORs of elements in $GF(2^M)$ which requires 2M two-input XOR gates. First, Δs is loaded into the autonomous LFSR

where its content is added componentwise modulo two with Δs^*. The shift in the autonomous LFSR and the count of the counter are controlled by the same clock signal. If $\alpha^{i-1}\Delta s=\Delta s^*$ for some i $(1\leq i\leq N)$, then the "stop count" signal is equal to one (indicating a match between $\alpha^{i-1}\Delta s$ and Δs^*), the counting stops and the counter's internal state indicates a faulty chip.

Example 1. We consider an example of a parallel compression-testing with the single-faulty-chip diagnostic capability for a system consisting of N=16 chips with M=16 outputs for every chip.

The space compressor implements a mapping of $\tilde{z}_i \rightarrow \tilde{z}_i H^T$ for i = 1,2,....,N, where H is the check matrix of the (16,14) Hamming code over $GF(2^{16})$. This matrix can be chosen in this case as

$$H = \begin{pmatrix} 1 & 1 & 1 & 1 & \cdots & 1 & 1 \\ 1 & \alpha & \alpha^2 & \alpha^3 & & \alpha^{14} & \alpha^{15} \end{pmatrix}. \qquad (7)$$

The realization of the space compressor using two chips is given in Fig. 4(a) and 4(b).

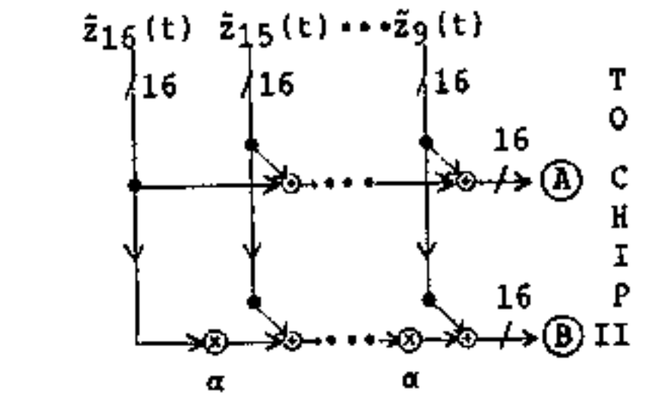

Fig. 4(a). The Space Compressor (Chip I)

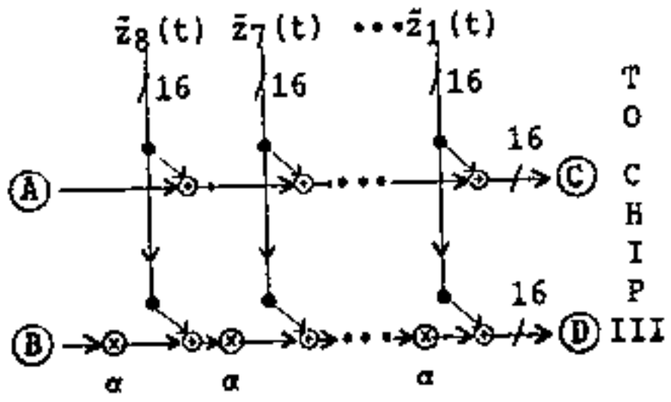

Fig. 4(b). The Space Compressor (Chip II)

Note that $\tilde{y}^*(t) = \tilde{z}_1(t)\oplus\alpha\tilde{z}_2(t)\oplus\alpha^2\tilde{z}_3(t)\oplus\ldots\oplus\alpha^{15}\tilde{z}_{16}(t)$, (correspond to the 2nd row of H (7)), is obtained by $\tilde{y}^*(t) = \tilde{z}_1(t) \oplus \alpha(\tilde{z}_2(t) \oplus \alpha(\tilde{z}_3(t) \oplus \alpha(\tilde{z}_4(t) \oplus \ldots \oplus \alpha(\tilde{z}_{15}(t)\oplus\alpha\tilde{z}_{16}(t))\ldots)))$.

The α-multiplier in Fig. 4 is a combinational circuit realizing a multiplication of element in $GF(2^M)$ by a primitive elements α which can be taken to be x if the irreducible polynomial p(x) used in the construction of $GF(2^M)$ is primitive [10]. The complexity of α-multiplier given in terms of a number of two-input XOR gates is equal to the number of terms x^i $(0<i<M)$ contained in the polynomial p(x) and denoted by w. A realiazation of α-multiplier in $GF(2^M)$ for M = 16 is shown in Fig. 5. In Fig. 5, the primitive polynomial of degree 16 over GF(2) is taken to be $p(x) = x^{16}\oplus x^{12}\oplus x^3\oplus x\oplus 1$. Then we have, $\gamma_{15}x^{15}\oplus\gamma_{14}x^{14}\oplus\ldots\oplus\gamma_0 \triangleq x(\beta_{15}x^{15}\oplus\ldots\oplus\beta_0) = \beta_{14}x^{15}\oplus\ldots\oplus(\beta_{11}\oplus\beta_{15})x^{12}\oplus(\beta_2\oplus\beta_{15})x^3\oplus\beta_1x^2\oplus(\beta_0\oplus\beta_{15})x\oplus\beta_{15}$. Therefore, the complexity of the α-multiplier is three two-input XOR gates which is equal to the number of nonzero terms x^i $(0<i<16)$ in the polynomial p(x), (w=3).

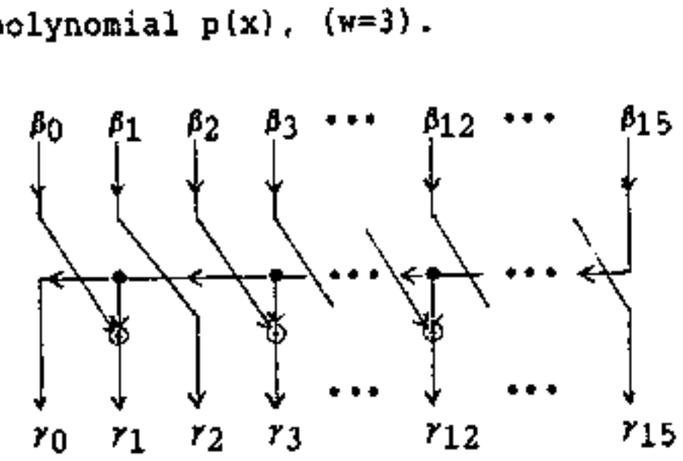

Fig. 5. Realiazation of α-Multiplier in $GF(2^{16})$

The time compressor consists of the two parallel-input LFSRs (see Fig. 2) separately connected to the outputs C and D of the space compressor (redundant chip II, see Fig 4). The feedback polynomial $p(x)=x^{16}\oplus x^{12}\oplus x^3\oplus x\oplus 1$ for both LFSRs is the same as in the realization of α-multiplier given by Fig.5.

In conclusion, for this example, the overall block diagram of the redundant components consists of three chips where the space compressor is realized by chip I and II (Fig. 4 (a) and (b)) and the comparator/decoder is the redundant chip III which is shown in Fig. 3. □

From the above example, one can see a drastic decrease in the hardware overhead for the proposed diagnostic technique by the space-time signature analysis when compared to the straightforward technique using N separate LFSRs, comparators, and references (see also Tables 1, 2 and 3 below in Section 4). The redundant circuitry is implemented by three additional chips. (Original board consists of 16 chips). Comparative analysis of overhead for the presented diagnostic techniques will be given in Section 4.

3 Serial Diagnosis (Transferring of Test Responses Via System Bus) by LFSRs

In this section we present a design for time compressors when the responses are serially transferred via system bus. The approach to the solution will be again based on single-error-correcting codes over $GF(2^M)$. This approach will not require wiring of outputs of the chips on the board to the time compressor and will not require a combinational space compressor. However, it will result in a considerable slowdown of a diagnostic process compared to the parallel diagnostic approach.

The proposed serial diagnosis is based on a nonbinary cyclic Hamming code where the response of the board-under-test, $\tilde{z}(t) = (\tilde{z}_N(t),\tilde{z}_{N-1}(t),\ldots,\tilde{z}_1(t))$, for every test pattern applied at moment t, $0\leq t\leq T-1$, is sequentially compressed into two M-

bit intermediate signatures. These signatures are the space signatures $\{\tilde{y}(t)\}$ and $\{\tilde{y}^*(t)\}$, t=0,1,...,T-1, mentioned previously for the parallel diagnostic technique. However, since the response of the board-under-test are serially transferred to the compressor, the space signatures are obtained by a sequential circuit.

Let $\tilde{z}(t)$, t=0,1,...,T-1, be transferred to the compressor in the following order:

$\tilde{z}_N(0),\tilde{z}_{N-1}(0),...,\tilde{z}_1(0),\ \tilde{z}_N(1),...,\tilde{z}_1(1),\ ...\ ,$
$\tilde{z}_N(T-1),...,\tilde{z}_1(T-1).$

To compute the space signature $\tilde{y}(t) = \tilde{z}_N(t) \circledast \tilde{z}_{N-1}(t) \circledast ... \circledast \tilde{z}_1(t)$, an M-bit T-flip-flop register is used. This is done by serially loading $\tilde{z}_i(t)$, i=N,N-1,...,1, to the M-bit T-flip-flop register.

To compute serially $\tilde{y}^*(t) = \alpha^{N-1}\tilde{z}_N(t) \circledast \alpha^{N-2}\tilde{z}_{N-1}(t) \circledast ... \circledast \tilde{z}_1(t)$ an LFSR with the feedback polynomial being the primitive polynomial p(x) considered in the definition of $GF(2^M)$ is used. This LFSR (see Fig. 2) is characterized by the linear recurrence where the next state is equal to the present state multiplied by the primitive element α added modulo two with the present input. It is easy to verify that the final state of this parallel-input LFSR with zero initial state is $\tilde{y}^*(t)$ when inputs are applied in the following order: $\tilde{z}_N(t),\tilde{z}_{N-1}(t),...,\tilde{z}_1(t)$.

Let us describe now the overall serial board-level diagnostic procedure which differs from the parallel diagnosis only with respect to the computation of space signatures.

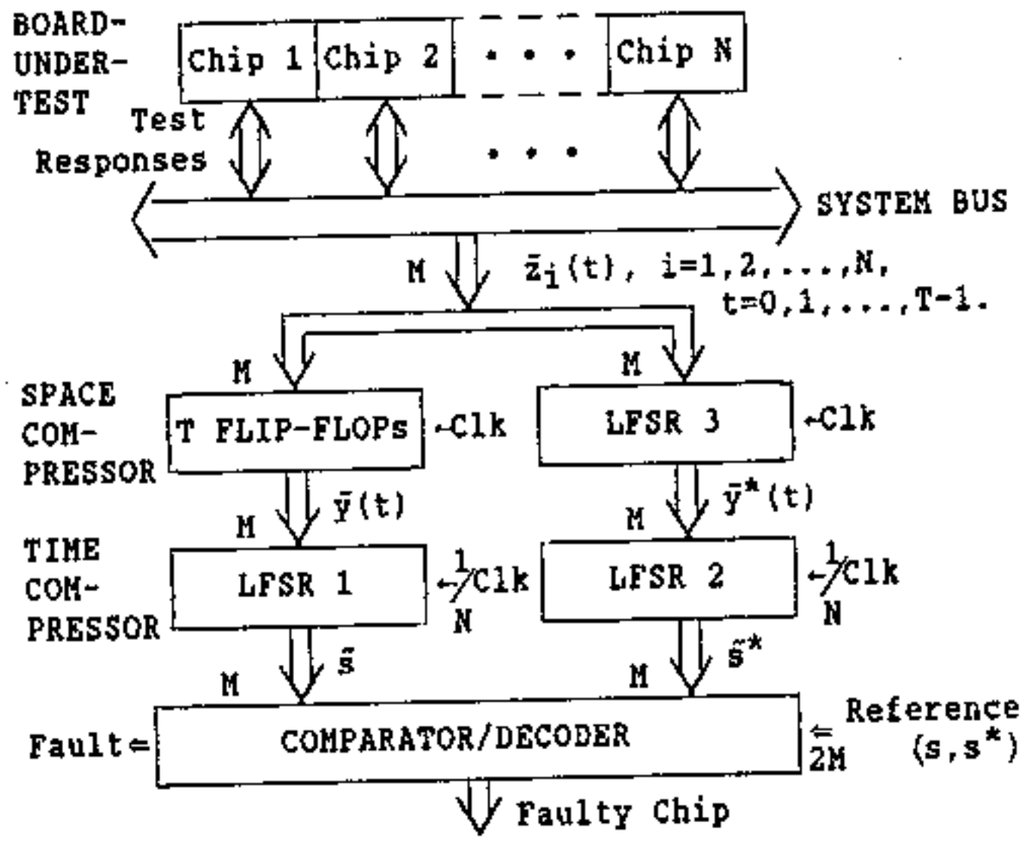

Fig. 6. Serial Board-Level Diagnosis by Signature Analysis

In Fig. 6, at a moment t, $0 \le t \le T-1$, test responses $\tilde{z}_i(t)$, i=N,N-1,...,1, are transferred to the redundant chip via system bus. The T-flip-flop (T-FF) register and LFSR 3 have been previously cleared. Responses, $\tilde{z}_i(t)$, i=N,N-1,...,1, are serially loaded into the T-FF register and LFSR 3 simultaneously. After $\tilde{z}_1(t)$ is clocked in, $\tilde{y}(t)$ and $\tilde{y}^*(t)$ are clocked into LFSR 1 and LFSR 2 (time compressor) respectively. Next, the T-FF register and LFSR 3 are cleared and the compression of $\tilde{z}_i(t+1)$, i=N,N-1,...,1, starts. When all T test patterns are applied to the board-under-test and the compression of $\tilde{z}(T-1)$ is done, signatures $\tilde{s}$ and $\tilde{s}^*$ are obtained and the faulty chip is located by the comparator and the decoder, previously described in Section 2.2.

4 Hardware Complexity of Board-Level Diagnosis

Let N be the number of chips on the board, M be the number of output lines per chip, w be the number of nonzero terms x^i $(0<i<M)$ in the primitive polynomial p(x) defining $GF(2^M)$ and M is the size of signatures. One can determine the hardware complexities of board-level diagnosis in terms of N, M and w as follows.

(i) The space-time compressor for parallel diagnosis requires three M-bit parallel-input LFSRs, two M-bit registers storing references s and s^* and a counter modulo N. The combinational space compressor requires 2M(N-1) + w(N-1) equivalent two-input gates and the comparator requires 4M-1 equivalent two-input gates. Assuming that a flip-flop requires eight two-input gates, we have for a hardware complexity of the redundant chips for parallel diagnosis

$$L_p(N,M,w) = 2MN+wN+8\lceil\log_2 N\rceil+51M+2w-1$$

equivalent two-input gates. (8)

We note that, the straightforward approarch for parallel diagnosis (using separate LFSR, comparator and reference storage register for each chip) requires N(21M + w - 1) equivalent two-input gates. Hence, the hardware overhead of the proposed parallel diagnosis is less than the straightforward approach as illustrated in Table 1 (rows 1 and 3) and in Table 2 (row 1).

(ii) The presented serial diagnosis (when responses from each chip are transferred via system bus) requires four M-bit parallel-input LFSRs, one M-bit T-FF register, two M-bit registers storing references s and s^*, and a counter modulo N. The total hardware overhead is given by,

$$L_s(M,N,w) = 8\lceil\log_2 N\rceil+61M+3w-1$$

equivalent two-input gates. (9)

The straightforward approarch to the serial diagnosis requires: an LSFR, a comparator, an M×1 multiplexer, a modulo N counter and N reference storage registers, total of $10MN+12M+(N+8)\lceil\log_2 N\rceil+w-N-1$ equivalent two-input gates. Thus, the proposed serial diagnosis requires less hardware overhead as N increases (see Table 1, rows 2 and 4, and Table 2, row 2).

Approach \ N	8	16	24	32	64
1. Parallel diagnosis by built-in LFSR for every chip	2,704	5,408	8,112	10,816	21,632
2. Serial diagnosis by testing each chip separately via system bus	1,514	2,834	4,170	5,482	10,802
3. Parallel diagnosis by Space-time compressor	1,125	1,445	1,701	1,981	3,109
4. Serial diagnosis by Space-time compressor	1,008	1,016	1,024	1,024	1,032

Equivalent two-input gate counts (one flip-flop is equivalent to eight gates).

Table 1. Overheads for Different Numbers of Chips N on the Board for M = 16 Outputs Per Chip

Comparison of Approaches \ N	8	16	24	32	64
Parallel Diagnosis	58%	73%	79%	82%	85%
Serial Diagnosis	33%	64%	75%	81%	90%

Table 2. Savings in Overheads for The Proposed Approaches for Boards with N chips and 16 Outputs per Chip

5. The Error-Masking Probabilities

With the single-faulty-chip model one can see that error sequences manifesting themselves as input sequences to LFSR 1 and LFSR 2 are multiples of each other in $GF(2^M)$ for both board-level diagnostic techniques presented. If an error sequence is compressed to zero (error-masking event) by LFSR 1 then any multiple of such error sequence will also be compressed to zero by LFSR 2, since LFSR 1 and LFSR 2 are identical. Hence, assuming equally probable error sequences, the error-masking probabilties (the probabilities that an error sequence is compressed to zero) for a single-chip-fault can be estimated as 2^{-M}. We note also, that for both techniques the error-masking probabilities given that faults occured in more than one chip is 2^{-2M}.

6. Conclusions

Board-level diagnostic techniques by signature analysis based on single-error-correcting Hamming codes over $GF(2^M)$ (where M is the number of outputs per chip) were presented. The parallel diagnosis, when responses from N chips on the board are wired to the compressor, was shown to provide a single-faulty-chip diagnostic capability. The space compressor consists of a decoder of a Hamming code with block size of N symbols and two redundant symbols over $GF(2^M)$. The time compressor consists of two M-bit parallel-input LFSRs separately compressing (in time) the outputs of the space compressor. A faulty chip on the board-under-test can be located by simple analysis of distortions in the obtained signatures. For the case of serial diagnosis (test responses from each chip are transferred to the compressor via system bus), we presented a technique for board-level dianosis based on serial computation of space signatures. The sequential circuit obtaining the space signatures consists of the T-FF register and a parallel-input LFSR.

Both presented board-level diagnositic techniques require less hardware than the straightforward approaches to parallel ans serial board-level diagnosses and hence offer efficients method for a design of BIST boards and for manufacturing testing.

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