

Recent Developments in Applications of Spectral Techniques in Logic Design and Testing of Computer Hardware ¹

by M. Karpovsky, IEEE Senior Member
Boston University, Boston, MA 02215, USA.

1 Historical Survey.

The first workshop on Spectral Techniques was conducted in Boston, October 1983. The workshop was devoted to the two major topics: applications of spectral techniques and fault detection. The workshop was attended by 35 people from 7 countries: USA, Canada, UK, West Germany, India, Australia and Peoples Republic of China. Thirteen invited papers were presented.

The following topics have been discussed at the workshop [1]:

- applications of spectral techniques for logic design and computer architecture (6 papers).
 - applications of spectral techniques for testing of computer hardware (2 papers).
 - applications of spectral techniques in digital signal processing and filtering (8 papers).
- Four papers have been devoted to testing and self-testing of computer hardware and to data compression of test responses.

Nine papers presented at the workshop have been selected for the publication as separate chapters in "Spectral Techniques and Fault Detection" (M. Karpovsky, editor), Academic Press, 1985 [2]. All these papers have been expanded to make them self-contained chapters in the book and reviewed by at least four reviewers. The list of the chapters included in the volume is given below:

- Introduction, by M. Karpovsky, Boston University.

¹This work was partially supported by NSF under the grant DCR-8317763.

- "Synthesis of Encoded PLA's ", by R. J. Lechner and A. Moezzi, University of Lowell, USA.
- "Spectral Processing of Switching Functions using Signal-Flow Transformations", by Ph. W. Besslich, University of Bremen, West Germany.
- "The Chrestenson Transform in Pattern Analysis", by C. Moraga and K. Seseke, Universitat Dortmund, West Germany.
- "Filtering in Communication Channel by Fourier Transforms over Finite Groups", by E. A. Trachtenberg, Drexel University and M. Karpovsky, Boston University, USA.
- "3D Cellular Arrays for Parallel Cascade Image/Signal Processing", by M. J. Corinthios, Ecole polytechnique de Montreal, Montreal, Canada.
- "Universal Testing of Computer Hardware", by M. Karpovsky and L. B. Levitin, Boston University, USA.
- "Techniques for Fault Detection in Combinational Logic", by D. M. Miller, University of Manitoba and J. C. Muzio, University of Victoria, Canada.
- "Signature Techniques in Fault Detection and Location", by S. J. Upadhyaya and K. K. Saluja, University of Newcastle, Australia.
- "The Design and Analysis of High Speed Logic", by G. R. Redinbo, University of California, Davis, USA.

In addition to these ten chapters the volume contains a complete (618 items) bibliography on applications of spectral techniques in logic design, testing and digital signal processing.

This volume in combination with older books by M. Karpovsky [3], S.L. Hurst [4] and the new book by S.L. Hurst, J. Muzio and M. Miller [5] presents a most comprehensive study on applications of spectral techniques in logic design and testing of computer hardware. It also complements two previous books by N. Ahmed and K. R. Rao [6] and K. Beauchamp [7] on applications of spectral techniques in digital signal processing.

2 Applications of Spectral Techniques to Logic Design

In this section we present a survey of some applications of spectral techniques (in particular of the Walsh Transform) for logic design. These design techniques may be used, for example, for design of CMOS gate arrays.

Let $f = f_i(x_0, \dots, x_{m-1})$ ($i = 0, \dots, k-1$) be a system of Boolean functions which have to be implemented by a gate array.

It is well-known [3, ch.1; ch.2; 8] that adding XOR gates (which have simple implementation in CMOS technology) to the standard NAND, NOR primitives results in considerable savings in gate counts of corresponding gate arrays.

The following three structures (Fig 1 - Fig 3), implementing this approach, have been investigated.

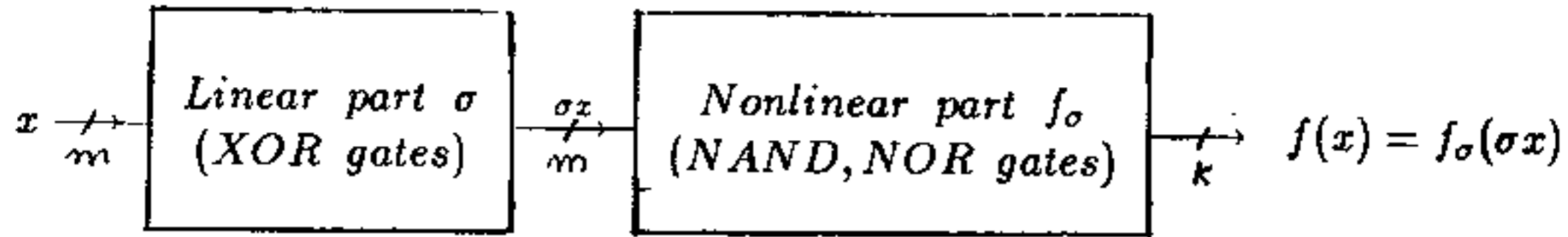


Fig 1. Serial Linearization (Domain Encoding)

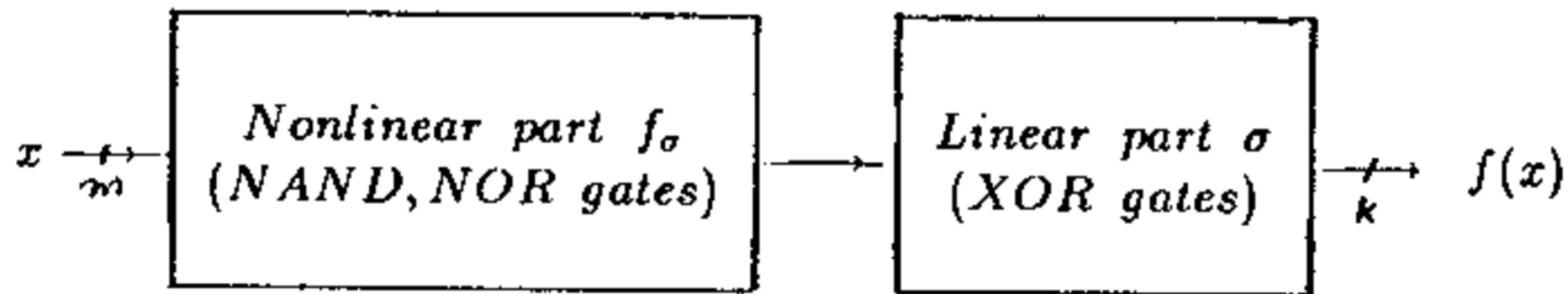


Fig 2. Serial Linearization (Range Decoding).

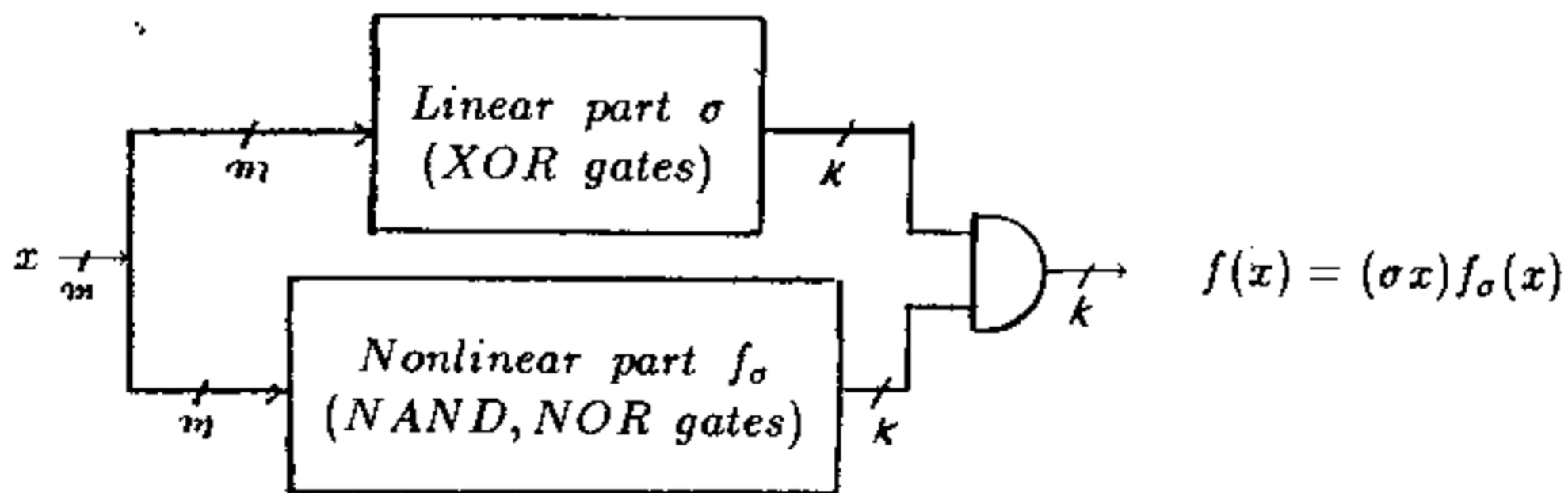


Fig 3. Parallel Linearization.

As a complexity criterion for a nonlinear part one can take

$$L(f) = \sum_{i=0}^{k-1} \sum_{d(X,Y)=1} f_i(X)f_i(Y), \quad (1)$$

where $d(X, Y)$ is the Hamming distance between binary m -vectors X and Y .

Justifications for the choice of this complexity criterion can be found in [3, ch.2; 2, ch.1]. Minimization problems for complexities of nonlinear parts for implementations of Fig 1 are known as problems of linearization of systems of Boolean functions, [3, ch.2; 8, 9].

It was shown [3, ch.2; 2, ch.1] that implementations of Fig 2 and Fig 3 for most cases do not generate considerable savings in gate counts.

The solution of the linearization problem (see Fig 1) with respect to criterion (1) is based on the total autocorrelation function, which can be defined in the following way:

$$B(\tau) = \sum_{i=0}^{k-1} \sum_X f_i(X)f_i(X \oplus \tau). \quad (2)$$

Let M be the set of all nonsingular $(m \times m)$ binary matrices over $GF(2)$; $T \in M$ and t_0, \dots, t_{m-1} are the columns of T , $T = (t_0, \dots, t_{m-1})$;

$$B(T) = \sum_{j=0}^{m-1} B(t_j). \quad (3)$$

Then [3, ch.2] $\sigma \in M$ minimizing the complexity $L(f_\sigma)$ of nonlinear part for Fig 1 is the inverse over $GF(2)$ of \tilde{T} , where

$$\max_{T \in M} B(T) = B(\tilde{T}). \quad (4)$$

The generalization of this algorithm for linearization of systems of multivalued functions can be found in [8; 9].

To compute the autocorrelation function we used the Weiner-Khinchin theorem for the Wash transform by applying twice the Fast Walsh transform [3, ch.1].

The computation of $\tilde{T} \in M$, defined by (4), is very time-consuming. To simplify this process we used the following observations.

Denote by $\rho(m)$ a probability that a randomly chosen binary $(m \times m)$ matrix $T = (t_{ij})$, ($\text{prob} \{t_{ij} = 1\} = 0.5$ for $i, j = 0, 1, \dots, m-1$) is nonsingular over $GF(2)$. Then

$$\rho(m) = \frac{\prod_{i=0}^{m-1} (2^m - 2^i)}{\prod_{i=0}^{m-1} (2^m - i)} \quad (5)$$

and

$$\lim_{m \rightarrow \infty} \rho(m) = \rho = 0.288788\dots \quad (6)$$

Since $\rho(m)$ converges to $\rho = 0.288788\dots$ very fast as $m \rightarrow \infty$, on average about one out of four randomly chosen $(m \times m)$ binary matrices is nonsingular over $GF(2)$.

To generate $\tilde{T} \in M$ using this observation we first generated $t_0, t_1, \dots, t_{5m-1}$ such that

$$B(t_i) \geq B(t_{i+1}) \quad (t_0 \neq 0; \quad i = 0, \dots, 5m - 2). \quad (7)$$

If $T_1 = (t_0, \dots, t_{m-1}) \in M$, then $\tilde{T} = T_1$. If $T_1 \notin M$ we construct $T_2 = (t_0, \dots, t_{m-1}, t_m)$; if $T_2 \in M$, then $\tilde{T} = T_2$, etc. This algorithm was implemented for system of Boolean functions of up to 22 arguments. Average savings in gate counts were about 25% without an increase in delays for the corresponding gate arrays.

It should be emphasized that this approach based on linearization may be less efficient for PLA implementations of nonlinear blocks (see Fig 1), since it may result in a considerable area overhead required to implement the linear part (see, [2, ch 1]).

3 Reed-Muller Transforms for Testing of Computer Hardware

Testing by verification of Walsh coefficients has been investigated in [17 - 19]. A good survey of spectral techniques for testing is presented in [2, ch.7].

For the Walsh transform every spectral coefficient depends on the values of a function of m arguments at all 2^m input vectors. This result in two major drawbacks of spectral testing techniques based on the Walsh transform. First, spectral testing requires 2^m steps, the same as for exhaustive testing. Second, since every spectral coefficient is an m -bit number, testing requires an additional m -bit counter.

In [10 - 15] spectral techniques for testing by the Walsh transform have been modified to reduce a time complexity of the test. This approach is known as testing by linear checks. The linear checking approach has been efficiently used in [10] for a chip level testing, in [11] for microprocessor testing, in [12] for memory testing and in [13; 14; 15] for testing of software for numerical computations. Modifications of the linear checking approach have been also used for self testing in distributed multiprocessor systems computing numerical functions [16].

We will describe here a new spectral approach for testing, resulting in a simultaneous reduction of a testing time and a hardware overhead required for testing. This approach is based on the Reed-Muller (RM) transform defined below. For this approach every spectral coefficient $\hat{f}(W)$ depends only on $2^{\|W\|}$ values of the original function $f(X)$ ($\|W\|$ is the number of ones in W) and in addition to this $\hat{f}(W) \in \{0, 1\}$ for every W .

Thus, verification of $\hat{f}(W)$ will require application of $2^{\|W\|}$ test patterns and the corresponding signature will contain one bit only. It will be shown below and in [20], that this one-bit signature will be sufficient for detection of a very high percentage of stuck-at faults.

We will discuss here some basic results related to testing by verification of RM coefficients. The detailed presentation and proofs can be found in [20].

The RM transform $f \rightarrow \hat{f}$ can be defined in the following way.

Let $X = (x_0, \dots, x_{m-1})$, $W = (w_0, \dots, w_{m-1})$, ($x_i, w_j \in \{0, 1\}$), and

$$R_X(W) = \prod_{i=0}^{m-1} x_i^{w_i} \quad (\text{where } 0^0 = 1). \quad (8)$$

Then

$$\hat{f}(W) = \bigoplus_{X=0}^N R_W(X) f(X) = \bigoplus_{X \subseteq W} f(X), \quad (9)$$

$$f(X) = \bigoplus_{W=0}^N R_X(W) \hat{f}(W) = \bigoplus_{W \subseteq X} \hat{f}(W), \quad (10)$$

where \bigoplus stands for the modulo 2 addition, $N = 2^m - 1$, $X \subseteq W$ iff $x_i \leq w_i$ for $i = 0, 1, \dots, m-1$.

Computing $\hat{f}(W)$ for all W requires only $m \cdot 2^{m-1}$ two input XOR gates. The corresponding Fast RM transform described in [20].

The Reed-Muller expansions (although represented in a different form) have been widely used in logic design (see, eg. [21-28]) and in error correcting codes [29]. We note also that (9) and (10) are similar to the Mobius inversion formulas well-known in numbers theory [29].

The RM transform, defined by (9) and (10) has many remarkable properties, some of them similar to the properties of the Walsh transform. We will mention here only few basic ones.

1. For any $X = (x_0, \dots, x_{m-1})$, $W = (w_0, \dots, w_{m-1})$

$$\bigoplus_{W=0}^N R_X(W) = \begin{cases} 1, & X = (0, 0, \dots, 0); \\ 0, & \text{otherwise}; \end{cases} \quad (11)$$

$$\bigoplus_{X=0}^N R_X(W) = \begin{cases} 1, & W = (1, 1, \dots, 1); \\ 0, & \text{otherwise}; \end{cases} \quad (N = 2^m - 1) \quad (12)$$

$$R_X(W) R_X(\bar{W}) = \prod_{i=0}^{m-1} x_i. \quad (13)$$

2. For any X, Y, W

$$R_{X \wedge Y}(W) = R_X(W) R_Y(W), \quad (14)$$

$$R_X(W \vee V) = R_X(W) R_X(V). \quad (15)$$

where \wedge and \vee stands for componentwise AND and OR operations respectively.

3. For any $f(x_0, \dots, x_{m-1})$

$$\hat{f}(0, 0, \dots, 0) = f(0, 0, \dots, 0), \quad (16)$$

$$\hat{f}(1, 1, \dots, 1) = \bigoplus_{X=0}^N f(X). \quad (17)$$

4. If $\varphi(X) = f(X) \oplus \phi(X)$, then

$$\hat{\varphi}(W) = \hat{f}(W) \oplus \hat{\phi}(W) \quad (\text{linearity}). \quad (18)$$

5. If $\hat{\varphi}(W) = \hat{f}(W) \cdot \hat{\phi}(W)$, then

$$\varphi(X) = \bigoplus_{Y \vee Z = X} f(Y) \phi(Z) \quad (\text{convolution}). \quad (19)$$

Properties of the RM transform with respect to detection of terminal (input/output) faults are very similar to those of the Walsh transform, but of course, for the RM transform all spectral signatures are one bit wide.

A stuck-at fault at input line x_i can be detected by verification of $\hat{f}(W)$ iff $\hat{f}(W) = 1$ for a fault free device and $w_i = 1$ ($W = (w_0, \dots, w_{m-1})$). A bridging between lines x_i and x_j can be detected by verification of $\hat{f}(W)$ iff $\hat{f}(W) = 1$ for a fault-free device and $w_i \neq w_j$. for example, if $\hat{f}(1, 1, \dots, 1) = \hat{f}(N) = 1$, then all multiple terminal stuck-at faults can be detected by verification of $\hat{f}(N)$.

Thus, the problem of minimization of testing time for detection of all terminal stuck-at faults with any multiplicity can be formulated in the following way.

For a given $f(X)$ construct W^1, W^2, \dots, W^r such that: 1) $\hat{f}(W^j) = 1$ ($j = 1, \dots, r$); 2) for any $i = 1, \dots, m-1$ there exists $j \in \{1, \dots, r\}$ such that $w_i^j = 1$; 3) $\sum_{j=1}^r 2^{\|W^j\|} \rightarrow \min$. Some partial solutions of this problem are given in [20].

Kuhl and Reddy [30] have shown that $2m+4$ test patterns are sufficient to detect all terminal stuck-at faults with any multiplicity in a combinational network. Karpovsky and Levitin [2, ch.6] have shown that there exist standard universal tests with $2m-2$ test patterns for detection of all multiple terminal faults in almost all combinational networks. It is shown in [20] by the use of the RM transform that only $1.25m$ test patterns are sufficient to detect all multiple terminal stuck-at faults in almost all combinational devices as $m \rightarrow \infty$ (of course, these RM-based tests are not standard but device-oriented tests).

Some results related to detection of terminal faults in standard computer components and to detection of internal stuck-at faults by verification of RM coefficients are also given in [20]. We will present here only one important result concerning the sensitivity of RM coefficients to internal faults and a number of test patterns in a minimal test detecting all internal single stuck-at faults in a network implementing a given $f(x_0, \dots, x_{m-1})$.

If any single stuck-at fault in a network implementing $f(x_0, \dots, x_{m-1})$ causes a distortion of at most A RM spectral coefficients $\hat{f}(w_0, \dots, w_{m-1})$, then we have for a minimal number R of test patterns detecting all single stuck-at faults in the network

$$R \leq \sum_{i=0}^{\lceil \log_2(A+1) \rceil - 1} \binom{m}{i}. \quad (20)$$

Thus, networks with a low sensitivity of RM coefficients to internal faults have a good testability. To illustrate formula (20) let us consider detection of stuck-at faults at outputs of AND gates in a canonical Reed-Muller network [26]. Then any fault of this

type distorts only one spectral coefficient, $A = 1$, by (20) $R = 1$ and test pattern $(1,1,\dots,1)$ detects all single stuck-at faults at outputs of AND gates.

REFERENCES

- [1]. Proc. of the First Int. Workshop on Spectral Techniques and Fault Detection, Boston, MA, Oct. 1983.
- [2]. "Spectral Techniques and Fault Detection," edited by M. Karpovsky, Academic Press, 1985.
- [3]. M. Karpovsky, "Finite Orthogonal Series in Analysis and Design of Digital Devices," John Wiley, 1976.
- [4]. S. Hurst, "Logical Processing of Digital Signals," Crane Russak, New York, 1978.
- [5]. S. Hurst., D.M. Miller and J.C. Muzio, "Spectral Techniques in Digital Logic," Academic Press, 1985.
- [6]. N. Ahmed and K.R. Rao, "Orthogonal Transforms for Digital Signal Processing," Springer, NY., 1975.
- [7]. K.G. Beauchamp, "Walsh Functions and Their Applications," Academic Press, 1975.
- [8]. M. Karpovsky, "Harmonic Analysis Over Finite Commutative Groups in Linearization Problems for Systems of Logical Functions," Information and Control, vol. 33, pp.142-165, 1977.
- [9]. C. Moraga, "Comments on A Method of Karpovsky," Information and Control, Vol. 35, N3, pp.243-246, 1978.
- [10]. M. Karpovsky, "Error Detection in Digital Devices and Computer Programs with the Aid of Linear Recurrent Equations over Finite Commutative Groups," IEEE Trans. on Computers, C-26, No. 3, 1977, pp. 208-219.
- [11]. M. Karpovsky, and R.G. Van Meter, "A Practical Algorithm for Testing of Microprocessors," Proc. 1984 Design Automation Conference, Albuquerque, New Mexico, pp 196-202, 1984.
- [12]. M. Karpovsky, "Memory Testing by Linear Checks," IEE Proceedings, Vol.131, Pt. E, No. 5, pp. 158-168, 1984.

- [13]. M. Karpovsky, "Error Detection for Polynomial Computations," IEE J. Computers and Digital Tech. No. 2, pp. 49-56, 1979.
- [14]. M. Karpovsky, "Detection and Location of Errors by Linear Inequality Checks," Proc. IEE Vol. 129, N3, May 1982, pp. 86-92.
- [15]. N.Goel and M. Karpovsky, "Functional Testing of Computer Hardware Based on Minimization of Magnitude of Undetected Errors," Proc. IEE Vol 129, N5, Sep 1982, pp. 161-181.
- [16]. M. Karpovsky, "An Approach for Fault Detection and Fault Correction in Distributed Systems Computing Numerical Functions," IEEE Trans. on Computers, No. 12, Dec 1981.
- [17]. A. K. Susskind, "Testing by verifying Walsh coefficients," IEEE Trans. on Computers V. C-32, pp. 198-201, 1983.
- [18]. D. M. Miller and J. C. Muzio, "Spectral techniques for fault detection," Proc. 12th Intl. Symp. on Fault Tolerant Computing, 1982, pp. 152-158.
- [19]. J. C. Muzio, "Composite spectral and the analysis of switching circuits," IEEE Trans. on Computers, V. C-29, pp. 750-753, 1980.
- [20]. T. Damarla and M. Karpovsky, "Reed-Muller transform for fault detection," Second Intl. Symp. on Spectral Techniques and Fault Detection, Ecole Polytechnique de Montreal, Montreal, Canada.
- [21]. D.E.Muller, "Application of Boolean Algebra to switching circuit design and to error detection," IRE Trans. Electron. Computers., vol. EC-3, pp 6-12, Sep. 1954.
- [22]. I.S.Reed, "A class of multiple error correcting codes and the decoding scheme," IRE Trans. Inform. Theory, vol. IT-4, pp 38-49, Sep. 1954.
- [23]. L.T.Fisher, "Unateness properties of AND-EXCLUSIVE-OR Logic Circuits," IEEE Trans. Computers, vol. c-23, no.2, Feb 1974, pp 166-172.
- [24]. M.Davio, "Ring-Sum expansions of Boolean functions," in Proc. Symp. on Computers and Automata, Polytech. Inst. of Brooklyn Symp. Proc., vol. 21, pp. 411-418, April 1971.
- [25]. C.V.Ramamoorthy, "Procedures for minimisation of 'Exclusive-OR' and 'Logical-Equivalence' switching circuits," in 1965 IEEE Symp. on Switching Theory and Logical Design (Ann Arbor, Mich., Oct 6-8), pp. 143-149.
- [26]. S.M.Reddy, "Easily testable realisations for logic functions," IEEE Trans. Computers vol. c-21, pp. 1183-1188, Nov 1972.

- [27]. Chen.X, "The mapping of spectral coefficients and its application," *Computer Electronic Engineering* 9, pp 167-180 (1982).
- [28]. Wu.X., Chen.X and Hurst.S.L, "Mapping of Reed-Muller coefficients and the minimisation of Exclusive-OR switching functions," *Proc. IEE E-129*, pp. 15-20 (1982).
- [29]. F. J. MacWilliams and N. J. A. Sloane, "The Theory of Error Correcting Codes," North Holland, 1977.
- [30]. J. G. Kuhl and S. M. Reddy, "On the detection of stuck-at-faults," *IEEE Trans. on Computers*, C-27 (May 1978), pp. 467-469.