Detection and identification of input/output stuck-at and bridging faults in combinational and sequential VLSI networks by universal tests *

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Abstract. In this paper we present universal tests for detection or identification of single and multiple stuck-at and bridging faults in combinational and sequential VLSI networks.

Denote by $P(T, F, m, k, s)$ the fraction of all devices with m inputs, k outputs and s feedback lines such that all faults from a set F of possible faults are detected (respectively, identified) by test T. We say that T is a universal test detecting (identifying) all faults from F if $\lim_{m \to \infty} P(T, F, m, k, s) = 1$.

In this paper we consider single and multiple stuck-at and bridging faults at input or output lines. For these faults we construct corresponding universal tests T, estimate probabilities $P(T, F, m, k, s)$ of fault detection or identification and present lower and upper bounds for the minimum number $N(m, k, s)$ of test patterns in universal tests. Asymptotic optimality of the suggested universal tests is proved for the important case of single stuck-at and bridging faults.

We also present practical examples of devices and tests which illustrate the usefulness of the estimates of minimum numbers $N(m, k, s)$ of test patterns.

For the universal tests T proposed in this paper probabilities $P(T, F, m, k, s)$ of fault

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detection or identification converge to one very fast. This implies that these universal tests may be quite efficient either as a first step in a testing procedure or in the case when a broad spectrum of complex VLSI devices has to be tested.

Keywords. VLSI networks, detection and identification of stuck-at and bridging faults, faults at input/output lines, universal tests, asymptotically optimal tests.

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1. Introduction

Three approaches have been used for testing of computer hardware, namely gate-level testing, functional testing and random testing. For gate-level testing, input data for test generation consist of gate-level description of a device under test and of a class of possible faults. In the case of functional testing input data for testing are represented by a functional description of a device and of a class of faults. For random testing, test patterns are generated randomly. The costs of test generation for gate-level testing begin to be prohibitively high with the transition to VLSI technology. We should also mention that in this case the problem of generation of an optimal test is NP-hard [1,2] even for the case of single stuck-at faults.

For functional testing the costs of test generation for VLSI devices are still very high, especially when a broad spectrum of devices has to be tested. On the other hand, in many cases it is very difficult to estimate a fault coverage in the case of functional testing [8–12].

For random testing the cost of test generation is minimal but a number of test patterns (testing time) may be very high for VLSI devices [13–15].

A different approach to testing which may be considered as filling the gap between functional and random testing has been proposed in [3,4]. This approach is based on the idea of universal tests which are able to detect (or to identify) all the faults of a given class in almost all devices of a given complexity (a rigorous definition of this concept will be given in Section 2).

For universal testing, the input data for test generation consist of parameters of a device under test (e.g., numbers of input lines, output lines, flip-flops, etc.) and a description of a class of possible faults (e.g., stuck-at faults of a given multiplicity).

Universal tests can be used for almost all devices, which means that the fraction of devices such that universal tests are inefficient tends to 0 very fast with an increase of complexity of a device under test. It will be shown below that if a universal test cannot be used for a given device and a class of faults, then, with a probability very close to 1, addition of a few test patterns to the original universal test will be sufficient to detect all the faults of a given class.

Test generation is very simple for universal tests (sometimes it is even simpler than for random testing, since it does not require a random number generator) and on the other hand it is not difficult to estimate fault coverage for almost all devices of a given complexity. A number of test patterns for universal testing is, generally speaking, greater than for functional testing but less than for random testing. For example, for detection of single stuck-at faults at input lines of combinational adders, subtracters, decoders, shifters, adders-accumulators, etc. with m input lines universal testing, as well as functional testing, requires only 2 test patterns and random testing requires at least $\lceil \log_2 m \rceil$ test patterns (see Example 4.3, below); for detection of bridgings between any two input lines for these devices universal, as well as functional, testing requires $\lceil \log_2 m \rceil$ test patterns and for random testing at least $\lceil 2 \log_2 m \rceil$ test patterns are needed ($\lceil a \rceil$ is the smallest integer greater or equal to a).

Since interconnections between VLSI chips are in many cases less reliable than chips themselves [16,17,3,4], we consider in this paper detection and identification of single and multiple stuck-at and bridging faults at input/output pins in both combinational networks and networks with memory. (By a bridging with multiplicity l we mean a bridging between l lines; results we are going to present are valid for both AND- and OR-type bridgings [6,7].) We also note that universal tests detecting multiple faults at input/output lines will also detect a high percentage of internal faults in a device under test.

For each of the above-mentioned problems we present universal tests, estimate probabilities of fault detection (or identification) and estimate the minimum numbers of test patterns. Since detection of single faults is for many practical cases the most important problem, we shall prove the optimality of the corresponding universal tests.

Section 2 contains description of devices under consideration, definitions and notations. In Section 3 general results on probabilities of detection (or identification) of all faults from a given class are presented. In Section 4 these results are applied to combinational networks with respect to stuck-at and bridging faults at input lines. This provides a generalization of corresponding results in [3]. The case of sequential networks with stuck-at faults at input/output lines is considered in Section 5. In Sections 2–5 we assume that all 100% of faults from a given class F are to be detected by universal tests in almost all devices. In Section 6 we consider a weaker requirement, namely, that only a given fraction of faults in almost all devices has to be detected by universal tests. For this case we present estimations on the probability of detection of a fraction of faults by universal tests and minimal numbers of test patterns in the corresponding universal tests.

2. Definitions and notations

An arbitrary digital binary network with memory may be represented by a block-diagram of Fig. 1.

Here m is the number of input lines, k the number of output lines, and s the number of feedback lines (the number of binary memory cells). Such a device will be referred to as an (m, k, s)-device, so that an $(m, k, 0)$-device is a combinational circuit.

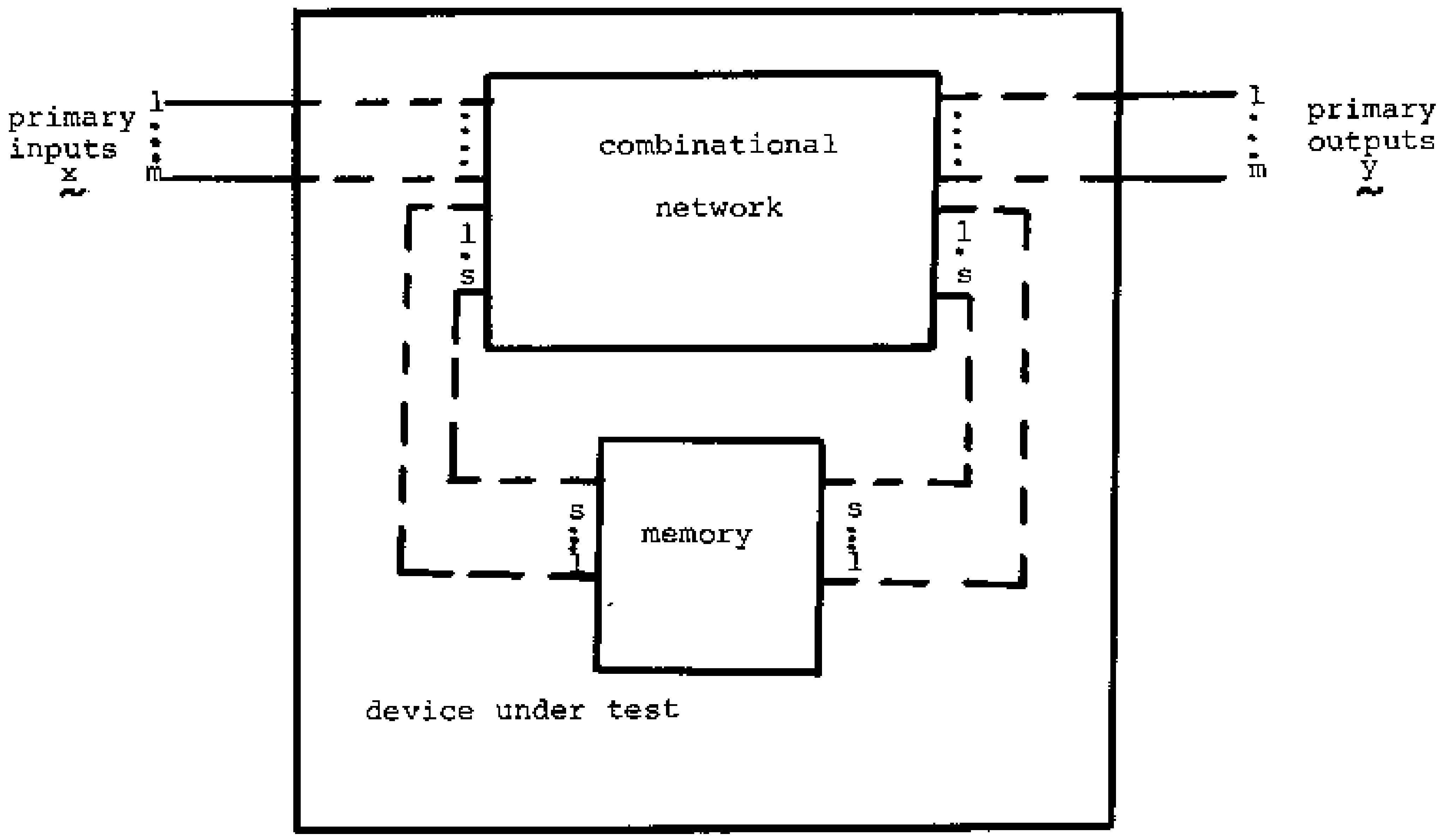

Fig. 1. Block-diagram of a network with memory.

Denote also (see Fig. 1) the following:

$x=(x_1,\ldots,x_m)$, the input binary vector,
$y=(y_1,\ldots,y_k)$, the output binary vector,
$z=(z_1,\ldots,z_s)$, the feedback binary vector,
$u=(u_1,\ldots,u_s)$, the memory output binary vector.

For a given device at discrete time τ, we have

$$y_j^{(\tau)}=y_j(x^{(\tau)},u^{(\tau)}) \quad (j=1,2,\ldots,k), \tag{1}$$

$$z_r^{(\tau)}=z_r(x^{(\tau)},u^{(\tau)}) \quad (r=1,2,\ldots,s), \tag{2}$$

where y_j and z_r are Boolean functions of $m+s$ variables, which are specified by the structure of the device and $u^{(\tau)}=z^{(\tau-1)}$. A test $T^{(m,N)}=(t^{(g)})$ is a sequence of N binary m-dimensional vectors $t^{(g)}=(t_1^{(g)},\ldots,t_m^{(g)})$, which are applied to the input lines of the device, vector $t^{(g)}$ being applied at the moment $\tau=g$ ($g=1,\ldots,n$). If a fault f occurs, the actual input vector $t^{(g)}(f)$ may be different from $t^{(g)}$. We say that the input vector is distorted if $t^{(g)}(f)\neq t^{(g)}$.

We denote by $Y^{(k,N)}=(y^{(1)},\ldots,y^{(N)})$ the sequence of output vectors produced by application to the device a sequence of test patterns $T^{(m,N)}=(t^{(1)},\ldots,t^{(N)})$, provided that the memory was cleared before testing.

For a fault-free device $Y^{(k,N)}$ is uniquely determined by $T^{(m,N)}$. However, if a fault f occurs in the device, $Y^{(k,N)}$ may depend on the fault $Y^{(k,N)}=Y^{(k,N)}(f)$. Denote by f_0 the situation when the device is fault-free.

Definition 2.1. It is said that test $T=T^{(m,N)}$ ($|T|=N$) *detects a fault* f in a given device, if for this device

$$Y^{(k,N)}(f)\neq Y^{(k,N)}(f_0). \tag{3}$$

Consider now a set of faults $F=\{f_w\}$, $w=0,1,\ldots,|F|-1$, which may occur in the device.

Definition 2.2. It is said that test $T=T^{(m,N)}$ *detects all the faults* from a set F in the device if for any $f_w\in F$, $w\neq 0$,

$$Y^{(k,N)}(f_w)\neq Y^{(k,N)}(f_0). \tag{4}$$

Definition 2.3. It is said that test $T=T^{(m,N)}$ *identifies* all faults from a set F in the device if for any $f_v, f_w\in F$, $v\neq w$,

$$Y^{(k,N)}(f_v)\neq Y^{(k,N)}(f_w). \tag{5}$$

Now let us consider the set of all (m,k,s)-devices for given m, k and s. Suppose that each one of these devices has the same probability of being chosen for testing; i.e., for an (m,k,s)-device under the test, the probability that the combinational part of the device (see Fig. 1) implements any given system of $k+s$ Boolean functions of $m+s$ arguments is $2^{-(k+s)2^{m+s}}$.

Denote by $P_{\det}(m, k, s)$ ($P_{\mathrm{id}}(m, k, s)$) a probability of detection (identification) of all faults by the given test in a randomly chosen (m, k, s)-device.

Definition 2.4. A sequence of tests ($T = T^{(m,N)}$) is called *universal for detection* (respectively, for identification) of all faults from a set $F = F(m, k, s)$, if

$$\lim_{m\to\infty} P_{\det}(m, k, s) = 1 \tag{6}$$

(respectively, if

$$\lim_{m\to\infty} P_{\mathrm{id}}(m, K, s) = 1). \tag{7}$$

(For the sake of simplicity we shall say also 'universal tests' instead of 'universal sequence of tests'.) The concept of universal sequence of tests is the central one in this paper. It is seen from Definition 2.4 that a performance of universal tests becomes the better, the larger are devices under test. This asymptotic property of universal tests makes this approach especially relevant for complex VLSI circuits.

The following notations will be used throughout the paper:

— l is the multiplicity of faults,

— $\hat{T}$ is the test matrix formed by test patterns of T as rows,

— $d_c(\hat{T})$ ($d_r(\hat{T})$) is the minimum Hamming distance [5] between columns (rows) of $\hat{T}$,

$$\alpha = \alpha(T, F) = \min_{f_v, f_w \in F} \frac{1}{N} \left|\left\{ g \mid t^{(g)}(f_v) \neq t^{(g)}(f_w) \right\}\right|, \tag{8}$$

— $N_{\det}(m, k, s)$ ($N_{\mathrm{id}}(m, k, s)$) is the asymptotic ($m \to \infty$) minimum number of test patterns in universal tests detecting (identifying) faults in (m, k, s)-devices,

— $\varepsilon(m)$ is an arbitrary function, such that $\varepsilon(m) \to \infty$ as $m \to \infty$.

The universal tests which are used in this paper for detection and identification of stuck-at faults in combinatorial networks will be constructed as follows. Let n be the maximum number, $n \leqslant m$, such that there exists a binary Hadamard matrix A_n of order n [5]. (It is known that Hadamard matrices exist for all multiples of 4 less than 268, and, very probably, for all multiples of 4.) Consider an $(n \times m)$ matrix A where the first n columns are those of A_n, and the last $m-n$ columns of A are the first $m-n$ columns of A_n. Let $a^{(h)}$ ($h = 1, 2, \ldots, n$) be the hth row of the matrix A. Then the test matrix $\hat{T}$ will consist of the rows

$$t^{(2g-1)} = a^{(g)}, \quad t^{(2g)} = \bar{a}^{(g)}, \qquad g = 1, 2, \ldots, \tfrac{1}{2}N, \tag{9}$$

where $N = |T| \leqslant 2n \leqslant 2m$ and $\bar{a}^{(g)}$ is the complement (negation) of $a^{(g)}$.

Example 2.5. Let $m = 11$, $N = 6$, then taking $n = 8$ and using (9) we obtain

$$\hat{T} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 \\ 0 & 0 & 0 & 0 & 1 & 1 & 1 & 1 & 0 & 0 & 0 \\ 1 & 1 & 1 & 1 & 0 & 0 & 0 & 0 & 1 & 1 & 1 \\ 0 & 0 & 1 & 1 & 0 & 0 & 1 & 1 & 0 & 0 & 1 \\ 1 & 1 & 0 & 0 & 1 & 1 & 0 & 0 & 1 & 1 & 0 \end{bmatrix}.$$

It follows from the properties of Hadamard matrices that the minimum Hamming distance between two distinct test patterns is

$$d_r(\hat{T}) \geqslant \tfrac{1}{2}n \geqslant \tfrac{1}{2}(m-3).$$

We shall restrict ourselves to stuck-at and bridging faults of multiplicity at most l ($l \leqslant \frac{1}{4}m - 1$). In this case $t^{(g)}(f_v) \neq t^{(h)}(f_w)$ for any $f_v, f_w \in F$, $g \neq h$. For detection and identification of stuck-at faults in sequential (m, k, s)-devices we will use universal tests of the following form:

$$(t^{(1)}, \ldots, t^{(N)}) = \Big((0, 0, \ldots, 0), (1, 1, \ldots, 1), (1, 0, \ldots, 0), (0, 1, \ldots, 1), \ldots,$$

$$\big(\underbrace{0, \ldots, 0}_{i}, 1, 0, \ldots, 0\big), \big(\underbrace{1, \ldots, 1}_{i}, 0, 1, \ldots, 1\big)\Big)$$

$$\text{where } N = 2i + 2. \tag{10}$$

The order of the test patterns, defined by (10), becomes essential for networks with memory.

3. Estimation of probabilities of fault detection and identification

In this section we present general results on lower bounds for probability $P_{\text{det}}(m, k, s)$ of detection and probability $P_{\text{id}}(m, k, s)$ of identification of all the faults from a given set F.

Theorem 3.1. (i) *Let F be a set of any input stuck-at or bridging faults of multiplicity at most l in combinational $(m, k, 0)$-circuits. Then, for any test T such that* $d_r(\hat{T}) \geqslant 2l + 1$,

$$P_{\text{det}}(m, k, 0) \geqslant (1 - 2^{-\alpha N k})^{|F|-1}, \tag{11}$$

$$P_{\text{id}}(m, k, 0) \geqslant (1 - 2^{-\alpha N k})^{\binom{|F|}{2}}. \tag{12}$$

(ii) *Let F be a set of single stuck-at faults at input lines of sequential (m, k, s)-devices. Then for a test T, defined by* (10),

$$P_{\text{det}}(m, k, s) \geqslant \left[1 - 2^{-0.5Nk}\left(2^{-s} + (1 - 2^{-s})2^{-k}\right)^{0.5N}\right]^{2m} \tag{13}$$

and

$$P_{id}(m, k, s) \geqslant \left[1 - 2^{-0.5Nk}\left(2^{-s} + (1-2^{-s})2^{-k}\right)^{0.5N}\right]^{\binom{2^m+1}{2}}. \qquad (14)$$

Proof. (i) Denote by B_m the set of all Boolean functions of m arguments ($|B_m| = 2^{2^m}$). Let $\varphi \in B_m$, then we have, for the probability $\Pr\{y_j = \varphi\}$ that the jth output of the device implements φ,

$$\Pr\{y_j = \varphi\} = 2^{-2^m}.$$

Let $(\varphi_0, \varphi_1, \ldots, \varphi_{2^m-1})$ be a binary vector. Then

$$\Pr\{y_j(0,\ldots,0,0) = \varphi_0, \ldots, y_j(1,\ldots,1,1) = \varphi_{2^m-1}\} = 2^{-2^m}.$$

Thus, for any $j = 1,\ldots,m$, $\{y_j(x) \mid x \in \{0,1\}^m\}$ [$\{0,1\}^m$ is the set of all binary m-vectors] is a set of independent random binary variables. For any $x^{(1)}, x^{(2)} \in \{0,1\}^m$,

$$\Pr\{y_j(x^{(1)}) = y_j(x^{(2)})\} = 0.5.$$

A fault $f \in F$ at input lines of a combinational device results in a distortion of a test pattern $t = t(f_0)$ into $t(f)$ [$d(t(f_0), t(f)) \leqslant l$, d is the Hamming distance]. Since, for our test T, $d_r(\hat{T}) \geqslant 2l+1$, we have

$$t^{(g)}(f_v) \neq t^{(h)}(f_w) \quad \text{for any } t^{(g)}, t^{(h)} \in T\ (g \neq h) \text{ and any } f_v, f_w \in F. \qquad (15)$$

For any fixed $f \in F$ ($f \neq f_0$) and $t = t(f_0) \in T$, if $t(f) \neq t(f_0)$, then $y_j(t(f_0))$ and $y_j(t(f))$ are independent binary variables. Thus,

$$\Pr\{y_j(t(f_0)) = y_j(t(f)) \text{ for all } t \in T\} \leqslant 2^{-\alpha N}.$$

Since, by definition, random variables $\{y_j\}$ are independent, we now have, for a probability $\lambda_{det}(m, k, 0)$ of detection of any given fault $f \in F$ ($f \neq f_0$) by test T,

$$\begin{aligned}\lambda_{det}(m,k,0) &= \Pr\{\exists j \in \{1,\ldots,k\}, \exists t \in T: y_j(t(f_0)) \neq y_j(t(f))\}\\ &= 1 - \Pr\{y_j(t(f_0)) = y_j(t(f))\ \forall t \in T, j = 1,\ldots,k\}\\ &\geqslant 1 - 2^{-\alpha N k}.\end{aligned}$$

In view of (15), events $\exists j$: $y_j(t(f_0)) \neq y_j(t(f))$ are independent for all $f \in F$, thus

$$P_{det}(m,k,0) = (\lambda_{det}(m,k,0))^{|F|-1} \geqslant (1 - 2^{-\alpha N k})^{|F|-1}.$$

To prove (12) we fix $f_v, f_w \in F (f_v \neq f_w)$. If $t(f_v) \neq t(f_w)$, then

$$\Pr\{y_j(t(f_v)) \neq y_j(t(f_2))\} = 0.5,$$

and, by (8),

$$\Pr\{y_j(t(f_v)) = y_j(t(f_w)) \text{ for all } t \in T\} \leqslant 2^{-\alpha N}.$$

Thus, we have for probability $\lambda_{id}(m, k, 0)$ that any two faults f_v and f_w produce different outputs ($Y^{(k,N)}(f_v) \neq Y^{(k,N)}(f_w)$):

$$\lambda_{\text{id}}(m, k, 0) = \Pr\{\exists j, t: y_j(t(f_v)) \neq y_j(t(f_w))\} \geq 1 - 2^{-\alpha Nk},$$

and, in a view of (15),

$$P_{\text{id}}(m, k, 0) = (\lambda_{\text{id}}(m, k, 0))^{\binom{|F|}{2}} \geq (1 - 2^{-\alpha Nk})^{\binom{|F|}{2}}.$$

(ii) For sequential networks with single fault f at input lines (see Fig. 1) and test sequence $T = (t^{(1)}, t^{(2)}, \ldots, t^{(N)})$ we have

$$\begin{cases} y_j^{(\tau)}(f) = y_j(t^{(\tau)}(f), u^{(\tau)}(f)) & (j = 1, \ldots, k) \\ z_r^{(\tau)}(f) = z_r(t^{(\tau)}(f), u^{(\tau)}(f)), u_r^{(\tau)}(f) = z_r^{(\tau-1)}(f) & \\ & (\tau = 1, \ldots, N, r = 1, \ldots, s), \end{cases}$$

where, for any $\varphi_i, \ldots, \varphi_k \in B_{m+s}$ and any $\psi_1, \ldots, \psi_s \in B_{m+s}$,

$$\Pr\{y_1 = \varphi_1, \ldots, y_k = \varphi_k\} = 2^{-k2^{m+s}}$$

and

$$\Pr\{z_1 = \psi_1, \ldots, z_s = \psi_s\} = 2^{-s2^{m+s}}.$$

We also note that, for any $j \in \{1, \ldots, k\}$ and $r \in \{1, \ldots, s\}$,

$$\{y_j(x, u) \mid x \in \{0, 1\}^m, u \in \{0, 1\}^2\}$$

and

$$\{z_r(x, u) \mid x \in \{0, 1\}^m, u \in \{0, 1\}^s\}$$

are sets of independent random binary variables.

For input stuck-at faults and test sequence $T = (t^{(1)}, t^{(2)}, \ldots, t^{(N)})$, defined by (10), for any two single input faults f_v, f_w either $t^{(2g-1)}(f_v) \neq t^{(2g-1)}(f_w)$ or $t^{(2g)}(f_v) \neq t^{(2g)}(f_w)$ for all $g = 1, 2, \ldots, \frac{1}{2}N$. Let $t^{(h)}(f_v) \neq t^{(h)}(f_w)$. Then

$$\Pr\{y_j^{(h)}(f_v) = y_j^{(h)}(f_w) \text{ for all } j = t, \ldots, k\} = 2^{-k} \tag{16}$$

and

$$\begin{aligned} &\Pr\{y_j^{(h+1)}(f_v) = y_j^{(h+1)}(f_w) \text{ for all } j = 1, \ldots, k\} \leq \\ &\quad \leq \Pr\{z_r^{(h+1)}(f_v) = z_r^{(h+1)}(f_w) \text{ for all } r = 1, \ldots, s\} \\ &\qquad + 2^{-k}(1 - \Pr\{\exists r \in \{1, \ldots, s\}: z_r^{(h+1)}(f_v) \neq z_r^{(h+1)}(f_w)\}) \\ &\quad = \Pr\{u^{(h)}(f_v) = u^{(h)}(f_w)\} + 2^{-k}(1 - \Pr\{u^{(h)}(f_v) \neq u^{(h)}(f_w)\}) \\ &\quad = 2^{-s} + 2^{-k}(1 - 2^{-s}). \end{aligned} \tag{17}$$

From (16) and (17) we have, for the probability of not detecting a fault f by two test patterns $t^{(h)}$, $t^{(h+1)}$,

$$\begin{aligned} &\Pr\{y_j^{(h)}(f_0) = y_j^{(h)}(f), y_j^{(h+1)}(f_0) = y_j^{(h+1)}(f) \text{ for all } j = 1, \ldots, k\} \leq \\ &\quad \leq 2^{-k}(2^{-s} + 2^{-k}(1 - 2^{-s})). \end{aligned}$$

Thus, we have for the probability $\lambda_{\text{det}}(m, k, s)$ of detection of any single input fault by the test sequence $(t^{(1)},\ldots,t^{(N)})$, defined by (10),

$$\lambda_{\text{det}}(m, k, s) \geqslant 1 - 2^{-0.5Nk}\left(2^{-s} + 2^{-k}(1 - 2^{-s})\right)^{0.5N},$$

and, for the probability $P_{\text{det}}(m, k, s)$ of detection of all single input stuck-at faults,

$$P_{\text{det}}(m, k, s) \geqslant \left(1 - 2^{-0.5Nk}\left(2^{-s} + 2^{-k}(1 - 2^{-s})\right)^{0.5N}\right)^{2m}.$$

Similarly, we have from (16) and (17) for the probability $\lambda_{\text{id}}(m, k, s)$ that any two different faults f_v and f_w produce different outputs:

$$\begin{aligned}\lambda_{\text{id}}(m, k, s) &= \\ &= 1 - \Pr\left\{ y_j^{(h)}(f_v) = y_j^{(h)}(f_w),\, y_j^{(h+1)}(f_v) = y_j^{(h+1)}(f_w),\, \forall j = 1,\ldots,k \right\} \\ &\geqslant 1 - \left(2^{-k}\left(2^{-s} + 2^{-k}(1 - 2^{-s})\right)\right)^{0.5N},\end{aligned}$$

and for the probability $P_{\text{id}}(m, k, s)$ of identification of all input single stuck-at faults in sequential networks

$$\begin{aligned}P_{\text{id}}(m, k, s) &= \left(\lambda_{\text{id}}(m, k, s)\right)^{\binom{2m+1}{2}} \\ &\geqslant \left(1 - 2^{-0.5Nk}\left(2^{-s} + 2^{-k}(1 - 2^{-s})\right)^{0.5N}\right)^{\binom{2m+1}{2}}. \quad \square\end{aligned}$$

4. Detection and identification of faults in combinational circuits

Consider now problems of detection and identification of stuck-at and bridging faults at inputs of combinational circuits with m input and k output lines.

Theorem 4.1. *If F is the set of all input stuck-at faults of multiplicity at most l ($l \leqslant \frac{1}{4}m - 1$) in combinational $(m, k, 0)$-devices, then tests $T = T^{(m,N)}$, defined by (9), form a universal sequence of tests for detection, if*

$$N = 2\left\lceil \left(\log_2 \sum_{i=1}^{l} 2^i \binom{m}{i} + \varepsilon(m)\right) \Big/ k \right\rceil, \tag{18}$$

and for identification, if

$$N = 2\left\lceil \left(2 \log_2 \sum_{i=0}^{l} 2^i \binom{m}{i} + \varepsilon(m)\right) \Big/ k \right\rceil, \tag{19}$$

for any $\varepsilon(m)$ such that $\varepsilon(m) \to \infty$ when $m \to \infty$.

Proof. For input stuck-at faults and universal tests $T = T^{(m,N)}$, $\alpha = 0.5$, $d_r(\hat{T}) \geqslant 2l + 1$ and $|F| = \sum_{j=0}^{l} 2^j \binom{m}{j}$. If N is defined by (18) (or by (19)), then the right-hand side of (11) (or (12)) converges to one as $m \to \infty$, for any k. Theorem 4.1 now immediately follows from Theorem 3.1. $\square$

Corollary 4.2 (i) *The asymptotical upper bounds on the minimum numbers of test patterns in universal sequences of tests for detection and identification of all the faults from F are, respectively,*

$$N_{\text{det}}(m,k,0) \lesssim 2\left\lceil \left(\log_2 \sum_{i=1}^{l} 2^i \binom{m}{i}\right)\Big/k \right\rceil, \tag{20}$$

$$N_{\text{id}}(m,k,0) \lesssim 2\left\lceil \left(2\log_2 \sum_{i=0}^{l} 2^i \binom{m}{i}\right)\Big/k \right\rceil. \tag{21}$$

(ii) *For detection of all single input stuck-at faults*

$$N_{\text{det}}(m,k,0) \sim 2\lceil(\log_2 m)/k\rceil. \tag{22}$$

(We denote $a(m) \lesssim b(m)$, if $\lim_{m\to\infty} a(m)/b(m) \leqslant 1$, and $a(m) \sim b(m)$, if $a(m) \lesssim b(m)$ and $a(m) \gtrsim b(m)$).

Proof. Formulas (20) and (21) follow from (18), (19) with $m \to \infty$. The lower bound

$$N_{\text{det}}(m,k,0) \geqslant 2\lceil(\log_2 m)/k\rceil$$

for the case of single faults has been proven in [3]. Formula (22) now follows from (20) with $l = 1$. □

It follows from (20) that

$$N_{\text{det}}(m,k,0) \lesssim \begin{cases} 2\lceil(l/k)\log_2 m\rceil & \text{if } b = 0, \\ 2\lceil(m/k)(b + H(b))\rceil & \text{if } b > 0, \end{cases} \tag{23}$$

where $b = \lim_{m\to\infty} l/m$, and $H(b) = -b\log_2 b - (1-b)\log_2(1-b)$ is the binary entropy function.

Thus, the minimum numbers of test patterns increase at most linearly with the number of input lines and decrease inversely proportionally with the number of output lines. If $k/m \gtrsim b + H(b)$, then, for large m, two test patterns $t^{(1)} = (0,\dots,0)$ and $t^{(2)} = (1,\dots,1)$ detect all stuck-at faults of multiplicities $l \lesssim bm$ in almost all devices.

Example 4.3. Consider detection and identification of input stuck-at faults in an m-input decoder. In this case $k = 2^m$, and all faults are detected and identified by universal tests $T^{(m,2)}$, consisting of two test patterns $t^{(1)} = (0,\dots,0)$ and $t^{(2)} = (1,\dots,1)$ only, which agrees with Corollary 4.2.

We note that universal tests $T^{(m,2)}$ can also be used for detection of single stuck-at faults in adders, subtractors, shifters, comparators, parity checkers, etc. If we use a random test for detection of single input stuck-at faults, then we have, for the probability $\Pr(m, N)$ that in every column of $\hat{T}$ there exist at least one '1' and at least one '0',

$$\Pr(m, N) = (1 - 2 \times 2^{-N})^m, \tag{24}$$

and $\lim_{m\to\infty} \Pr(m, N) = 1$ only if $N \gtrsim \log_2 m$. (We suppose that for random tests every input vector may be taken as a test pattern with probability 2^{-m}.) Thus, for all these devices, detection of single stuck-at faults by universal tests requires two test patterns and by random tests at least $\log_2 m$ test patterns.

A lower bound on the fault detection probability for input stuck-at faults can be easily obtained from Theorem 3.1, taking into account that for the test defined by (9) we have $\alpha = 0.5$. One can see that this probability converges to 1 very fast with the increase of the number of test patterns N (see Fig. 2).

Now we shall turn to the detection of bridgings in combinational circuits. Denote by $n(m, d)$ the length of a shortest binary error-correcting code V with the Hamming distance dist $V = d$ such that V contains at least m codewords, and all columns of a generating matrix of V are different. Upper and lower bounds for $n(m, d)$ are well known [5].

Theorem 4.4. *If F is the set of all input bridgings with multiplicity at most l, where $l < 2^{\lfloor \log_2 m \rfloor - 2}$, then*

(i) *any sequence of test $T = T^{(m,N)}$ such that*

$$d_c(\hat{T})k - \log_2 \sum_{i=2}^{l} \binom{m}{i} \to \infty \quad \left(\text{or } d_c(\hat{T})k - 2\log_2 \sum_{i=2}^{l} \binom{m}{i} \to \infty \right)$$

when $m \to \infty$, (25)

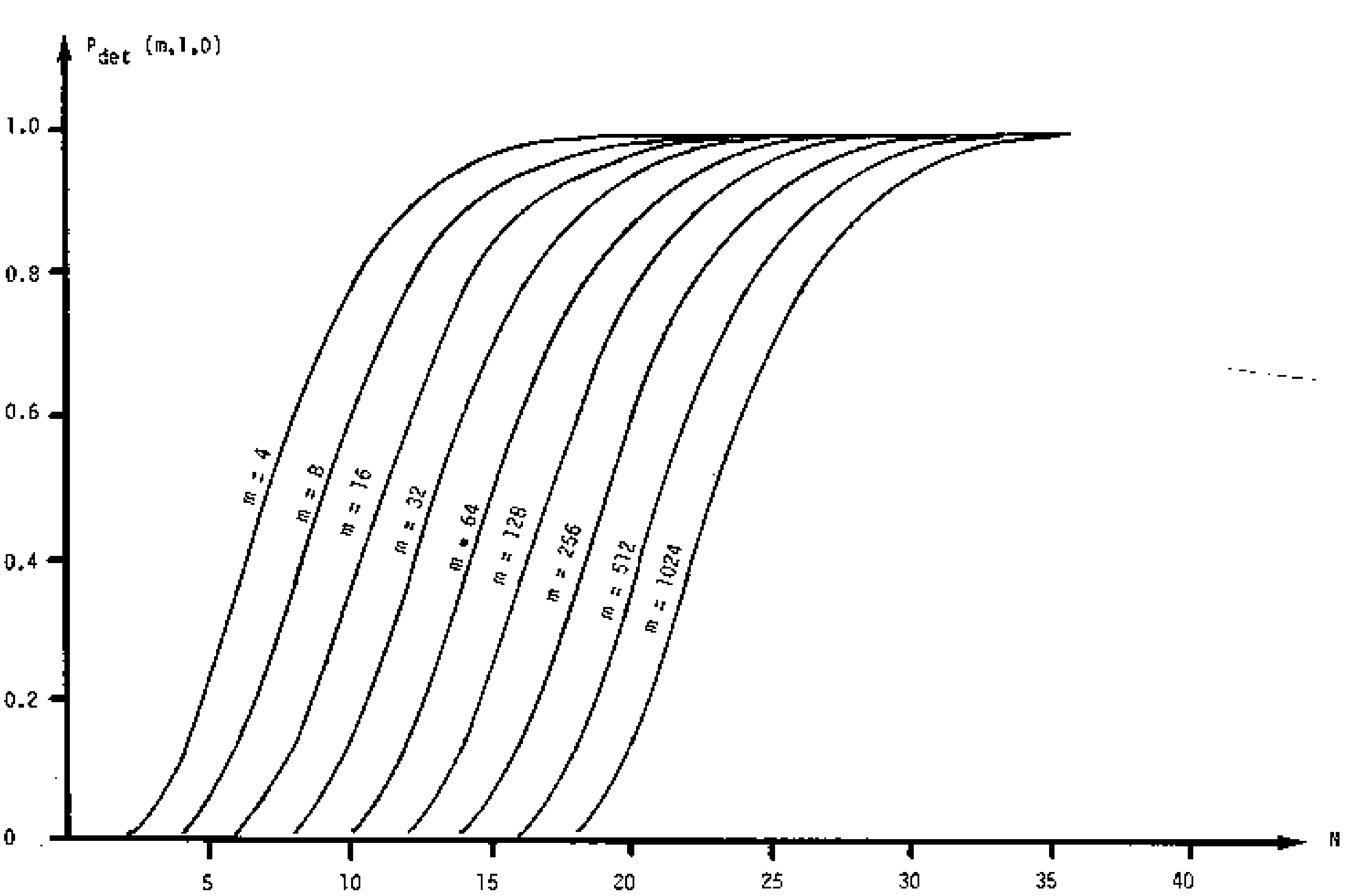

Fig. 2. The probability of detection of single input stuck-at faults in combinational (m 1, 0)-devices as a function of a number of test patterns.

is the universal sequence of tests detecting (or identifying) all these bridgings,

(ii) *for detection and identification of input bridgings with multiplicity at most* l

$$N_{\text{det}}(m, k, 0) \leq n\left(m, \left\lceil \frac{1}{k} \log_2 \sum_{i=2}^{l} \binom{m}{i} \right\rceil\right)$$

and

$$N_{\text{det}}(m, k, 0) \leq n\left(m, \left\lceil \frac{1}{k} \log_2 \sum_{i=2}^{l} \binom{m}{i} \right\rceil\right), \tag{26}$$

(iii) *if* $l/k \to 0$, *then*

$$N_{\text{det}}(m, k, 0) \sim N_{\text{id}}(m, k, 0) \sim \log_2 m. \tag{27}$$

($\lfloor a \rfloor$ *is the greatest integer less or equal to* a).

Theorem 4.4 is a generalization of results presented in [3,4] on detection of bridgings between two input lines.

Proof. (i) For bridgings between input lines, columns of a matrix $\hat{T}$ are different codewords of a code V with $|V| \geqslant m$, dist $V = d_c(\hat{T})$ and $\alpha N = \alpha|T| = d_c(\hat{T})$. Since in this case $|F| = 1 + \sum_{j=2}^{l}\binom{m}{j}$ and $d_r(\hat{T}) \geqslant 2l + 1$, we have, from (11) and (25),

$$\lim_{m \to \infty} P_{\text{det}}(m, k, 0) \geqslant \lim_{m \to \infty} \left(1 - 2^{d_c(\hat{T})k}\right)^{\sum_{j=2}^{l}\binom{m}{j}} = 1.$$

Similarly, we have from (12) and (25)

$$\lim_{m \to \infty} P_{\text{id}}(m, k, 0) = 1.$$

(ii) Condition (25) is satisfied iff

$$\text{dist } V = d_c(\hat{T}) \geqslant \left\lceil \left(\log_2 \sum_{j=2}^{l} \binom{m}{j} + \varepsilon(m)\right) / k \right\rceil$$

(or iff

$$\text{dist } V = d_c(\hat{T}) \geqslant \left\lceil \left(\log_2\left(1 + \sum_{j=2}^{l} \binom{m}{j}\right) + \varepsilon(m)\right) / k \right\rceil).$$

Asymptotical upper bounds (26) now follow from the definition of $n(m, d)$.

(iii) To prove the lower bound it is sufficient to note that for detection of input bridgings all columns of $\hat{T}$ have to be different. Thus,

$$N_{\text{id}}(m, k, 0) \geqslant N_{\text{det}}(m, k, 0) \geqslant \lceil \log_2 m \rceil.$$

To prove the upper bound we note that, for $l/k \to \infty$ and $m \to \infty$,

$$n\left(m, \left\lceil \frac{2 \log_2\left(1 + \sum_{j=2}^{l}\binom{m}{j}\right) + \varepsilon(m)}{k} \right\rceil\right) \sim$$

$$\sim n\left(m, \left\lceil \frac{\log_2 \sum_{j=2}^{l}\binom{m}{j} + \varepsilon(m)}{k} \right\rceil\right)$$

$$\sim \log_2 m. \qquad \square$$

Example 4.5. Consider detection of bridging faults in an m-bit decoder ($k = 2^m$). In this case $l/k \to 0$ with $m \to \infty$, and any test with distance

$$d_c(\hat{T}) = \left\lceil (1/k) \log_2 \sum_{i=2}^{l} \binom{m}{i} \right\rceil = 1$$

between columns of $\hat{T}$ detects all input bridgings. We can take, for example, the test matrix which columns are binary representations of the numbers 0, 1,..., $m-1$. Then, obviously, $N = \lceil \log_2 m \rceil$.

The same universal test with $N = \lceil \log_2 m \rceil$ can be used for detection of all bridgings between two input lines for adders, subtractors, multipliers, etc. If we use a random test, then we have, for the probability $\Pr(m, N)$ that all columns of $\hat{T}$ are different,

$$\Pr(m, N) = \prod_{i=1}^{m-1} (1 - i2^{-N})^m, \tag{28}$$

and $\lim_{m\to\infty}\Pr(m, N) = 1$ only if $N \gtrsim \lceil 2 \log_2 m \rceil$. Thus, for these devices, detection of input bridgings by universal tests requires $\lceil \log_2 m \rceil$ test patterns and for random tests at least $\lceil 2 \log_2 m \rceil$ test patterns.

As one can see from Theorems 4.1 and 4.4, identification of stuck-at faults in combinational circuits requires twice as many test patterns as their detection, while identification of bridgings for $l/k \to 0$ requires asymptotically the same number of test patterns as detection.

5. Detection and identification of stuck-at faults in circuits with memory

This section is devoted to the problem of detection and identification of single stuck-at faults at primary inputs for a device with a block-diagram represented by Fig. 1.

Note that introduction of memory in a device may result only in a decrease of a number of test patterns required for detection (or identification) of input stuck-at faults. Indeed, some input faults which distort test patterns but not distort primary output vectors at time g may distort information in memory, and this may result in distortions of primary output vectors at time $g+1$, $g+2$, etc. In fact, as is shown below,

$$N_{\text{det}}(m, k, s) \leq N_{\text{det}}(m, k, 0) \leq 2N_{\text{det}}(m, k, s)$$

and (29)

$$N_{\text{id}}(m, k, s) \leq N_{\text{id}}(m, k, 0) \leq 2N_{\text{id}}(m, k, s),$$

where the lower bounds are achieved for small s and the upper bounds for large s. For detection of input stuck-at faults, test sequences, defined by (10), will be used. In contrast with the previous case, the order of test patterns is essential for devices with memory. We start with a lower bound for the minimum number of test patterns for detection of single input stuck-at faults.

Suppose that for a single stuck-at fault f at a primary input and for a sequence of test patterns $(t^{(g)}, t^{(g+1)},\dots,t^{(g+\tau)})$ test pattern $t^{(g)}$ is distorted by $f(t^{(g)}(f) \neq t^{(g)})$ and $t^{(g+1)},\dots,t^{(g+\tau)}$ are not distorted $(t^{(i)}(f) = t^{(i)}, i = g+1,\dots,g+\tau)$. For this case denote by $q(\tau, k, s)$ the probability that the test sequence $(t^{(g)},\dots,t^{(g+\tau)})$ does not detect f. By definition $q(0, k, s) = 1$ for any k, s.

Lemma 5.1. *For any* $\tau \geqslant 0$,

$$q(\tau, k, s) = 2^{-s}(1-\gamma^{\tau})/(1-\gamma) + \gamma^{\tau}, \tag{30}$$

where

$$\gamma = 2^{-k}(1-2^{-s}). \tag{31}$$

Proof. If, for $t^{(g+1)},\dots,t^{(g+\tau)}$, fault f does not distort test patterns, it can only be detected as a result of distortion of data coming into the memory (see Fig. 1). If, for a test pattern $t^{(g+h)}$ $(h = 1,\dots,\tau)$, data coming into the memory are not distorted, then the same is true for any $t^{(g+r)}$ for $h \leqslant r \leqslant \tau$. Let us denote by γ the probability that, if a memory output vector is distorted, then, at the same moment τ, a primary output vector is not distorted and a memory input vector is distorted (i.e., distortion of data in memory is 'masked' at primary outputs). Then,

$$\gamma = \Pr\{y^{(\tau)}(f) = y^{(\tau)}, z^{(\tau)}(f) \neq z^{(\tau)} \mid u^{(\tau)}(f) \neq u^{(\tau)}\} = 2^{-k}(1-2^{-s}),$$

where $y^{(\tau)} = (y_1^{(\tau)},\dots,y_k^{(\tau)})$, $u^{(\tau)} = (u_1^{(\tau)},\dots,u_s^{(\tau)})$ and $z^{(\tau)} = (z_1^{(\tau)},\dots,z_s^{(\tau)})$ (see Section 2).

Denote by q_h the probability that fault f is not detected if all memory inputs at the moments g, $g+1,\dots,g+h-1$ are distorted $(z^{(g+i)}(f) \neq z^{(g+i)}, i = 0, 1, \dots, h-1)$ and a memory input vector at moment $g+h$ is not distorted $(z^{(g+h-1)}(f) = z^{(g+h-1)})$. Then $q_h = \gamma^{h-1}2^{-s}$ $(h = 1,\dots,\tau)$, and, by definition of q_h and $q(\tau, k, s)$, we have

$$q(\tau, k, s) = \sum_{h=1}^{\tau} q_h + \gamma^{\tau} = 2^{-s}(1-\gamma^{\tau})/(1-\gamma) + \gamma^{\tau}.$$

We note that $q(\tau, k, s)$ is monotonically decreasing with the increase of τ, i.e.,

$$\begin{aligned} &q(0, k, s) = 1, \qquad q(1, k, s) = 2^{-s} + 2^{-k}(1-2^{-s}), \\ &\lim_{\tau\to\infty} q(\tau, k, s) = 2^{-s}(1/1 - 2^{-k}(1-2^{-s})). \qquad \square \end{aligned} \tag{32}$$

Theorem 5.2. *If F is the set of all single input stuck-at faults, then*

$$N_{\det}(m, k, s) \geqslant 2\lceil\{\log_2 m + \varepsilon(m)\}/\{k - \log_2(2^{-s} + 2^{-k}(1-2^{-s}))\}\rceil. \tag{33}$$

Proof. For a minimal test T denote by $a_{0,j}$ ($a_{1,j}$) a number of zeros (ones) in the jth column of $\hat{T}$. We shall suppose, without loss of generality that $a_{0,j} \leqslant a_{1,j}$ ($a_{0,j} \leqslant \frac{1}{2}|T| = \frac{1}{2}N$).

Let us consider the stuck-at-1 fault at the jth input line. Denote by $t^{(i_r)}$ ($r = 1,\ldots,a_{0,j}$) test patterns from $T = (t^{(1)},\ldots,t^{(N)})$ which are distorted by this fault and $t^{(i_r+h)}$ ($h = 1,\ldots,\tau_r$, $r = 1,\ldots,a_{0,j}$) test patterns which are not distorted ($\sum_{r=1}^{a_{0,j}} \tau_r \leqslant N - a_{0,j}$). Then we have, for the probability $\lambda_j(k, s)$ that this fault is detected by T,

$$\lambda_j(k,s) = \left(1 - 2^{-ka_{0,j}} \prod_{r=1}^{a_{0,j}} q(\tau_r, k, s)\right). \tag{34}$$

It follows from (30) and (31) that

$$\min_{(\tau_1,\ldots,\tau_{a_{0,j}})} \prod_{r=1}^{a_{0,j}} q(\tau_r, k, s) \geqslant \left(q\left(\left\lceil \frac{N - a_{0,j}}{a_{0,j}} \right\rceil, k, s\right)\right)^{a_{0,j}}. \tag{35}$$

Thus, we have, from (34) and (35),

$$\lambda_j(k,s) \leqslant \left(1 - 2^{-ka_{0,j}}\left(q\left(\left\lceil \frac{N - a_{0,j}}{a_{0,j}} \right\rceil, k, s\right)\right)^{a_{0,j}}\right) \tag{36}$$

Since the right-hand side in (36) is monotonically increasing with the increase of $a_{0,j}$ and $a_{0,j} \leqslant \frac{1}{2}N$, we have from (36), (34) and (32), for the probability $P_{\text{det}}(m, k, s)$ that all single stuck-at faults are detected,

$$\begin{aligned} P_{\text{det}}(m,k,s) &\leqslant \prod_{j=1}^{m} \lambda_j(t,k,s) \leqslant \left(1 - 2^{-0.5kN}(q(1,k,s))^{0.5N}\right)^m \\ &= \left(1 - 2^{-0.5kN}(2^{-s} + 2^{-k}(1 - 2^{-s}))^{0.5N}\right)^m. \end{aligned} \tag{37}$$

The right-hand side of (37) converges to one only if (33) is satisfied. □

Let us now construct upper bounds for minimal numbers of test patterns for detection and identification of single input stuck-at faults.

Theorem 5.3. *If F is the set of single input stuck-at faults, then the tests $T = T^{(m,N)}$, defined by* (10), *form a universal sequence of tests for detection, if*

$$N = 2\left\lceil \{\log_2 m + \varepsilon(m)\} / \{k - \log_2(2^{-s} + (1 - 2^{-s})2^{-k})\} \right\rceil,$$

and for identification, if (38)

$$N = 2\left\lceil \{2\log_2 m + \varepsilon(m)\} / \{k - \log_2(2^{-s} + (1 - 2^{-s})2^{-k})\} \right\rceil.$$

Proof. For single input stuck-at faults in sequential networks and universal tests $T = T^{(m,N)}$, defined by (10), we have $\alpha = 0.5$ and $d_r(\hat{T}) \geqslant 2l + 1$. If N is defined by (38), then the lower bound (13) (or (14)) for a probability of fault detection (identification) converges to one as $m \to \infty$. Theorem 5.3 now immediately follows from Theorem 3.1. □

Corollary 5.4. *For detection and identification of single input stuck-at faults, we have*

$$N_{\text{det}}(m, k, s) \sim 2\lceil(\log_2 m)/\{k - \log_2(2^{-s} + (1-2^{-s})2^{-k})\}\rceil, \tag{39}$$

$$N_{\text{id}}(m, k, s) \lesssim 2\lceil(2\log_2 m)/\{k - \log_2(2^{-s} + (1-2^{-s})2^{-k})\}\rceil. \tag{40}$$

Proof. Formulas (39) and (40) follow from Theorems 5.2 and 5.3 with $m \to \infty$. □

One can see from (39) and (40) that the minimum number of test patterns depends on ratio of k and s. In particular,

$$N_{\text{det}}(m, k, s) \sim \begin{cases} 2\lceil(\log_2 m)/k\rceil & \text{if } 2/k \to 0, \\ 2\lceil(\log_2 m)/(2k)\rceil & \text{otherwise.} \end{cases} \tag{41}$$

Comparing (20) and (21) for $l = 1$ with (39) and (40), one can see that, for a small number of memory cells, numbers of test patterns for combinational and sequential circuits are asymptotically equal, but if $s \gtrsim k$, then the size of the test can be reduced by half.

Example 5.5. Consider detection of input stuck-at faults in an adder-accumulator with m input lines. In this case $k = s > m$, and the test $T^{(m,2)}$ with test patterns $t^{(1)} = (0,\ldots,0)$, $t^{(2)} = (1,\ldots,1)$ detects all faults, which agrees with Theorem 5.2.

A lower bound on the probability of detection of single input stuck-at faults is given by (13). One can see that this probability converges to 1 very fast with the increase of the number N of test patterns (see also Fig. 3).

Let us now briefly consider the problem of detection of faults at output lines. This problem was solved in [3] for combinational networks. It was shown, in particular, that for detection of all output stuck-at faults (of any multiplicity)

$$P_{\text{det}}(m, k, 0) = (1 - 2^{-N+1})^k \quad \text{for any } m. \tag{42}$$

Moreover, any sequence of tests with $N = \log_2 k + \varepsilon(k)$ is a universal one for $k \to \infty$, and

$$n_{\text{det}}(m, k, 0) \sim \log_2 k. \tag{43}$$

Similarly, for output bridgings of any multiplicity,

$$P_{\text{det}}(m, k, 0) = \prod_{i=0}^{k-1} (1 - i2^{-N}) \quad (\text{for any } m). \tag{44}$$

It follows from (44) that, when $k \to \infty$, any sequence $(T^{(m,N)})$ of tests such that

$$N = \lceil 2\log_2 k + \varepsilon(k)\rceil \tag{45}$$

is a universal one, and

$$N_{\text{det}}(m, k, 0) \sim 2\log_2 k. \tag{46}$$

It can be easily verified that expressions (42)–(46) remain valid for networks with memory as well. Moreover, since the primary outputs are the observation points,

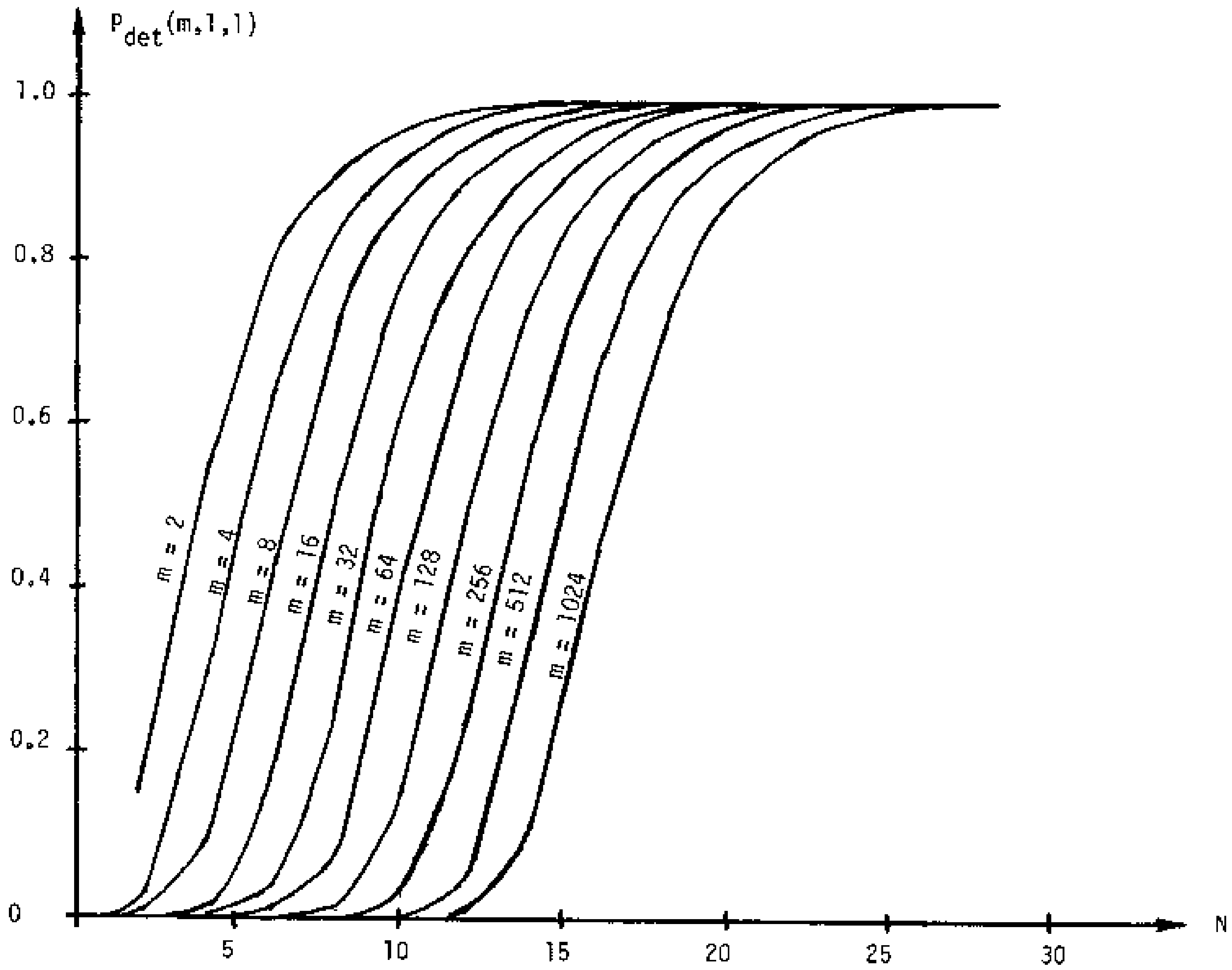

Fig. 3. The probability of detection of single output stuck-at faults in sequential $(m, 1, 1)$-devices as a function of a number of test patterns.

any test which detects output faults will also identify them. (For the reader's convenience we have summarized all results from Sections 4 and 5 in Table 1.)

6. Detection of a fraction of faults from a given class by universal tests

In previous sections we supposed that in almost all devices 100% of faults from a given class F are to be detected by universal tests. In this section we shall consider a weaker requirement that in almost all devices only at least $(1-\beta)|F|$ faults are to be detected, where $0<\beta<0.5$ and $|F|$ is the cardinality of F $(|F|\to\infty)$. In this case we shall use the same universal tests as in the previous sections. As we shall see below, for any constant $\beta>0$ the minimal number of test patterns $N_{\text{det}}^{(\beta)}(m, k, s)$ is not increasing with an increase of m. Let $P_{\text{det}}^{(\beta)}(m, k, s)$ be a probability of detection of $(1-\beta)|F|$ faults from the set F by the given test T in a randomly chosen (m, k, s)-device.

Theorem 6.1. (i) *Let F be a set of any input stuck-at or bridging faults with multiplicity at most l $(l \leqslant \frac{1}{4}m-1)$ in combinational $(m, k, 0)$-devices. Then for any*

Table 1

Upper bounds for minimal numbers $N_{det}(m, k, s)$ of test patterns for detection and identification of faults.

Type of network	Class F of faults	Upper bound for asymptotic-minimum number of test patterns	
		Detection	Identification
Combinational ($s = 0$)	Input single stuck-at	$2\left\lceil \frac{\log_2 m}{k} \right\rceil$ [a]	$2\left\lceil \frac{2\log_2 m}{k} \right\rceil$
	Input stuck-at with multiplicity at most l ($l \leqslant \frac{1}{4}m - 1$).	$2\left\lceil \frac{\log_2 \sum_{j=1}^{l} 2^j \binom{m}{j}}{k} \right\rceil$	$2\left\lceil \frac{2\log_2 \sum_{j=0}^{l} 2^j \binom{m}{j}}{k} \right\rceil$
	Input bridgings with multiplicity at most l ($l/k \to \infty$)	$\log_2 m$ [a]	$\log_2 m$ [a]
	Output stuck-at with any multiplicity	$\log_2 k$ [a]	$\log_2 k$ [a]
	Output bridgings with any multiplicity	$2\log_2 k$ [a]	$2\log_2 k$ [a]
Networks with memory ($s > 0$)	Input single stuck-at	$2\left\lceil \frac{\log_2 m}{k - \log_2(2^{-s} + 2^{-k}(1 - 2^{-s}))} \right\rceil$ [a]	$2\left\lceil \frac{2\log_2 m}{k - \log_2(2^{-s} + 2^{-k}(1 - 2^{-s}))} \right\rceil$
	Output stuck-at with any multiplicity	$\log_2 k$ [a]	$\log_2 k$ [a]
	Output bridgings with any multiplicity	$2\log_2 k$ [a]	$2\log_2 k$ [a]

[a] The corresponding tests are asymptomatically optimal.

test T such that $d_r(\hat{T}) \geqslant 2l+1$,

$$P_{\text{det}}(m, k, 0) \geqslant \sum_{i=0}^{\beta|F|} \binom{|F|}{i} (1-2^{-\alpha Nk})^{|F|-i} 2^{-\alpha Nki}. \tag{47}$$

For input stuck-at faults in combinational networks, we have

$$N_{\text{det}}^{(\beta)}(m, k, 0) \leqslant 2(1-(\log_2 \beta)/k) \tag{48}$$

and, for input bridging in combinational networks, we have

$$N_{\text{det}}^{(\beta)}(m, k, 0) \leqslant n(m, \lfloor 1-(\log_2 \beta)/k \rfloor) \tag{49}$$

($n(m, d)$ *has been defined in Section* 4).

(ii) *Let F be a set of single input stuck-at faults in sequential* (m, k, s)*-devices. Then for a test T, defined by* (10),

$$P_{\text{det}}^{(\beta)}(m, k, s) \geqslant \sum_{i=0}^{\beta|F|} \binom{|F|}{i} \left(1-2^{-0.5Nk}(2^{-s}+(1-2^{-s})2^{-k})^{0.5N}\right)^{|F|-i} \times 2^{-0.5Nki}(2^{-s}+(1-2^{-s})2^{-k})^{0.5Ni} \tag{50}$$

and

$$N_{\text{det}}^{(\beta)}(m, k, s) \leqslant 2\left[1-(\log_2 \beta)/\{k-\log_2(2^{-s}+(1-2^{-s})2^{-k})\}\right]. \tag{51}$$

Proof. Denote by $\lambda = \lambda(m, k, s)$ the probability of detection of any given fault $f \in F$ by test T. Then, by definition,

$$P_{\text{det}}^{(\beta)}(m, k, s) = \sum_{i=0}^{\beta|F|} \left(\binom{|F|}{i}\right) \lambda^{|F|-i}(1-\lambda)^i. \tag{52}$$

For input stuck-at or bridging faults in combinational devices we have, from Theorem 3.1,

$$\lambda = \lambda(m, k, 0) \geqslant 1-2^{-\alpha Nk} \quad \text{for any } m. \tag{53}$$

For single input stuck-at faults in sequential (m, k, s)-devices it follows from Theorem 3.1 that

$$\lambda = \lambda(m, k, s) \geqslant 1-2^{-0.5Nk}(2^{-s}+(1-2^{-s})2^{-k})^{0.5N}. \tag{54}$$

Formulas (45) and (50) now immediately follow from (52) and (53), (54). It follows from (52) that $P_{\text{det}}^{(\beta)}(m, k, s) \to 1$ iff $\beta > i-\lambda$ for $|F| \to \infty$.

Thus, in view of (53), if for a combinational device

$$\alpha N > -(1/k) \log_2 \beta, \tag{55}$$

then $\beta > 1-\lambda$ and $P_{\text{det}}^{(\beta)}(m, k, s) \to 1$ as $|F| \to \infty$. Formulas (48) and (49) now immediately follow from (55).

For sequential devices, if

$$N > -2(\log_2 \beta)/\{k-\log_2(2^{-s}+(1-2^{-s})2^{-k})\}, \tag{56}$$

then, in view of (54), $\beta > 1-\lambda$ and $P_{\text{det}}^{(\beta)}(m, k, s) \to 1$ as $|F| \to \infty$. □

We note that, if we are applying universal tests $T^{(m,N)}$ where $N = N_{\det}^{(\beta)}(m, k, s)$, then the probability λ of detection of any fault from F does not converge to one as $m \to \infty$, but we have $\lambda > 1 - \beta$. (In previous sections we always had $\lim_{m\to\infty} \lambda(m, k, s) = 1$.) As we can see from Theorem 6.1, minimum numbers of test patterns detecting any given fraction $1 - \beta$ $(0 < \beta < 0.5)$ of faults in almost all devices do not depend on multiplicity l of faults and for stuck-at faults do not depend on numbers of input lines m. (As we have seen in previous sections, for $\beta = 0$ minimum numbers of test patterns for detection of input stuck-at faults depend on m and l.)

Example 6.2. Let us estimate a minimum number of test patterns detecting 99% of input stuck-at faults in almost all devices. From (48) with $\beta = 0.01$ we have that at most 14 test patterns are sufficient for combinational networks (if $k \geqslant 7$, then two test patterns are sufficient). For sequential networks at most 12 test patterns will be sufficient (if $k - \log_2(2^{-s} + (1 - 2^{-s})2^{-k}) \geqslant 7$, then two test patterns are sufficient).

References

[1] Ibarra, A.K. and S. Sahni, Polynomially complete fault detection problems, *IEEE Trans. Comput.* **C-24** (1975) 242–248.

[2] Sahni, S. and A. Bhatt, The complexity of design automation problems, *Proc. 17th Design Automation Conf.*, Minneapolis (1980) pp. 402–411.

[3] Karpovsky, M.G., Universal tests for detection of input/output stuck-at and bridging faults, *IEEE Trans. Comput.* **C-32** (11) (1983).

[4] Karpovsky, M.G., Universal tests detecting input/output faults in almost all devices, *Proc. 1982 Internat. Test Conf.*, Cherry Hill, NJ, 1982.

[5] MacWilliams, F.J. and N.J.A. Sloane, *The Theory of Error-Correcting Codes* (North-Holland, Amsterdam, 1977).

[6] Mei, K.C.Y., Bridging and stuck-at faults, *IEEE Trans. Comput.* **C-23** (1974) 720–727.

[7] Kodandapani, K.L. and D.K. Pradhan, Undetectability of bridging faults and validity of stuck-at fault test set, *IEEE Trans. Comput.* **C-23** (1980) 55–59.

[8] Thatte, S.M. and J.A. Abraham, Test generation for microprocessors, *IEEE Trans. Comput.* **C-29** (N6) (1980) 423–441.

[9] Akers, S.B., Functional testing with binary decision diagrams, *8th Internat. Symp. on Fault-Tolerant Computing*, Toulouse (1978) pp. 75–82.

[10] Karpovsky, M.G., Error detection in digital devices and computer programs with the aid of linear recurrent equations over finite commutative groups, *IEEE Trans. Comput.* **C-26** (N3) (1977) 208–219.

[11] Karpovsky, M.G. and E.A. Trachtenberg, Linear checking equations and error-correcting capability of computation channels, *Proc. IFIP Congress 1977* (North-Holland, Amsterdam, 1977) pp. 619–624.

[12] Goel, N. and M.G. Karpovsky, Functional testing of computer hardware based on minimization of magnitude of undetected errors, *IEE Proc.* **129** (1982) 169–181.

[13] Rault, J.C., A graph theoretical and probabilistic approach to the fault detection of digital circuits, *Internat. Symp. on Fault-Tolerant Computing* (1971) pp. 16–29.

[14] David, R. and P. Thevenad-Fosse, Minimal detecting transition sequences: Application to random testing, *IEEE Trans. Comput.* **C-29** (N6) (1980) 514–518.

[15] Savir, J., G. Ditlow and P.H. Bardell, Random pattern testability, *Internat. Symp. on Fault-Tolerant Computing*, Milano, 1983.
[16] Weiss, C.D., Bounds on the length of terminal stuck-fault tests, *IEEE Trans. Comput.* **C-21** (1972) 305–309.
[17] Kuhl, T.G. and S.M. Reddy, On detection of terminal stuck-faults, *IEEE Trans. Comput.* **C-27** (1978) 467–469.