

Mark Karpovsky

Department of Electrical, Computer
and System Engineering
College of Engineering
Boston University, Boston, USA

It is well known that central problems in the design of computer hardware (e.g., minimization of systems of boolean functions, state assignment for sequential machines, test generation for logical networks, etc.) are NP-hard [1-3], this implies that any algorithm for the optimal solution of these problems will require an exponential number of steps. This is the same order of complexity as that of a 'brute-force' approach, which would compare all possible solutions. The situation becomes even more difficult when noting the dramatic increase in device complexity with the transition to very large scale integration (VLSI) technologies. Due to this difficulty, there is a growing demand for analytical design techniques useful for large and complex devices. This situation is similar to that in the design of optimal control systems. Here, the system is first linearized and then an optimal approximating linear system is designed by the use of such powerful techniques as the Laplace transform, the Fourier transform, or Z-transform. The spectral techniques presented in this book are similar to these classical transforms: in fact, they maintain the basic properties of the Laplace and Fourier transforms. They may be considered as digital realizations of these classical transforms for the analysis and design of digital devices, both binary and non-binary.

An intrinsic advantage of the Laplace and Fourier transforms is that many problems which are difficult to solve in the original or 'time' domain have simple solutions in the transform

respect to the spectral techniques discussed in this volume.

Consider a combinational network (Fig.1) with m binary input lines x_0, \dots, x_{m-1} and k binary output lines y_0, \dots, y_{k-1} . This device can be described by the function

$$y = f(x) \quad \left(x = \sum_{j=0}^{m-1} 2^j x_j, \quad y = \sum_{j=0}^{k-1} 2^j y_j, \quad x_j, y_j \in \{0,1\} \right). \quad (1)$$

Let us introduce now a transform $W: f \rightarrow \hat{f}$, as an analog to the Fourier transform, for the system f of Boolean functions:

$$\hat{f}(\omega) = 2^{-m} \sum_x f(x) W_\omega(x), \quad (2)$$

where $\omega = \sum_{j=0}^{m-1} 2^j \omega_j$ ($\omega_j \in \{0,1\}$) and

$$W_\omega(x) = W_x(\omega) = (-1)^{(x, \omega)} = (-1)^{\sum_{j=0}^{m-1} x_j \omega_j} \quad (3)$$

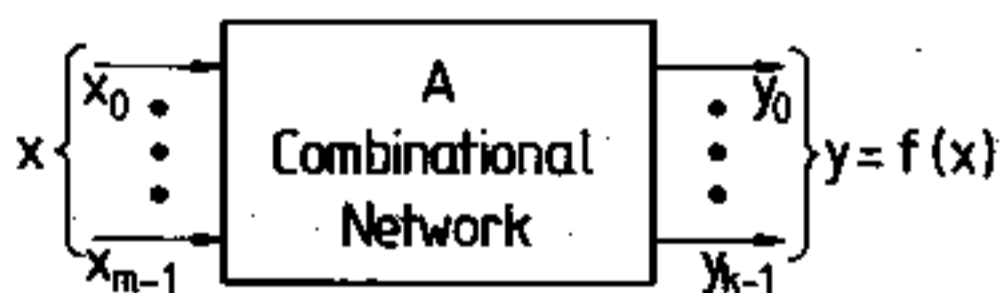


Fig. 1. Block diagram of a combinational network.

f is known as the Walsh transform or as the Walsh-Hadamard transform. A $(2^m \times 2^m)$ - matrix with elements $W_{x,\omega} = (-1)^{(x,\omega)}$ is called the Hadamard matrix.

The inverse Walsh transform $W^{-1}:\hat{f} \rightarrow f$ is defined by

$$f(x) = \sum_{\omega} \hat{f}(\omega) W_{\omega}(x) = \sum_{\omega} \hat{f}(\omega) (-1)^{(x,\omega)} \quad (4)$$

function $\hat{f}(\omega)$ is known as the Walsh image, or the Walsh spectrum, of the original function $f(x)$ and ω is called as a 'generalized frequency'.

There are quite a few important design problems that are difficult to solve using the original function $f(x)$, yet easy to solve using the spectrum $\hat{f}(\omega)$. Some of these problems will be considered in Chapters 1,2,3,4,5, and, 7 of this book.

Before we discuss applications of the Walsh transform, let us briefly review the basic properties of the Walsh functions and the Walsh transform. (For a more detailed description and proofs of the properties of the Walsh transform, see [5-7].)

First we note that the Walsh functions $\{W_{\omega}(x) = (-1)^{(x,\omega)}, (\omega_0, \dots, \omega_{m-1}), x = (x_0, \dots, x_{m-1})\}$ form a complete set of orthogonal functions, i.e.

$$2^{-m} \sum_x W_{\omega}(x) W_t(x) = \delta_{\omega,t} \quad (5)$$

$$\delta_{\omega,t} = \begin{cases} 1, & \omega = t \\ 0, & \omega \neq t \end{cases} \quad ; \text{ and if}$$

$$\sum_x f(x) W_{\omega}(x) = 0 \text{ for all } \omega, \text{ then } f(x) = 0 \text{ for all } x.$$

are related to the group structure of the set of binary vectors.

A set G is said to be a group with respect to operation $*$ iff: for any $a, b \in G$ we have $a*b \in G$, there exists $0 \in G$ such that $a*0=0*a=a$ for any $a \in G$, and for any $a \in G$ there exists $a^{-1} \in G$ such that $a*a^{-1} = a^{-1}*a=0$. A group G is said to be commutative (Abelian) if for any $a, b \in G$ $a*b=b*a$. Two groups, G_1 with operation $*$ and G_2 with operation o , are said to be isomorphic iff there exists a one-to-one mapping (isomorphism) $h:G_1 \leftrightarrow G_2$ such that $h(a*b)=h(a)oh(b)$ for any $a, b \in G_1$.

The set of Walsh functions form a multiplicative group

$$W_0(x) = 1 \quad \text{for all } x \text{ and}$$

$$W_\omega(x) W_t(x) = W_{\omega \oplus t}(x) , \quad (6)$$

where $\omega \oplus t$ is a componentwise modulo-2 addition (XOR operation) of binary n -vectors ω and t .

From (6) and (3) we also have the following 'translation of arguments' property

$$W_\omega(x \oplus \tau) = W_\omega(x) W_\omega(\tau) . \quad (7)$$

The most important property of Walsh functions is that the multiplicative group of Walsh functions is isomorphic to the dyadic group F_2^m of all binary m -vectors with respect to the componentwise XOR operation. The importance of this property follows from the fact that all logical functions describing behavior of combinational computer components are defined over the dyadic group F_2^m . This isomorphism, $h:W_\omega(x) \leftrightarrow \omega$, is similar to the isomorphism between the multiplicative group of the

exponential functions $\exp(i \frac{2\pi}{N} x\omega)$ ($i = \sqrt{-1}$) and the additive

group of integers $\{0, \pm 1, \pm 2, \pm 3, \dots\}$.

We shall summarize now the most important properties of the Walsh transform $W:f \rightarrow \hat{f}$ (i.e., of the harmonic analysis over the dyadic group) which will be widely used throughout this book.

$f(x) = \sum_{i=1}^s a_i f_i(x)$, where a_i are arbitrary real numbers.

$$\text{Then } \hat{f}(\omega) = \sum_{i=1}^s a_i \hat{f}_i(\omega) \quad (8)$$

Translation of Arguments

$\rho(x) = f(x \oplus \tau)$ for some $\tau \in F_2^m$.

$$\hat{\rho}(\omega) = W_\tau(\omega) \hat{f}(\omega) \quad (9)$$

Logical Convolution

Let $\rho = f_1 \otimes f_2$, for $\rho(\tau) = \sum_x f_1(x) f_2(\tau \oplus x)$. (10)

$$\widehat{f_1 f_2} = \hat{f}_1 \otimes \hat{f}_2 \quad (11)$$

$$2^{-m} \widehat{f_1 \otimes f_2} = \hat{f}_1 \hat{f}_2$$

Plancherel Theorem

$$2^{-m} \sum_x f_1(x) f_2(x) = \sum_\omega \hat{f}_1(\omega) \hat{f}_2(\omega) \quad (12)$$

Poisson Summation Theorem

Let V be a subgroup of the dyadic group F_2^m of binary m -tuples and V^\perp be the orthogonal subgroup

$$\{(x_0, \dots, x_{m-1}) \mid x_0 z_0 \oplus x_1 z_1 \oplus \dots \oplus x_{m-1} z_{m-1} = 0 \text{ for all } (z_0, \dots, z_{m-1}) \in V\}.$$

$$\sum_{x \in V} f(x) = \sum_{\omega \in V^\perp} f(\omega) \quad (13)$$

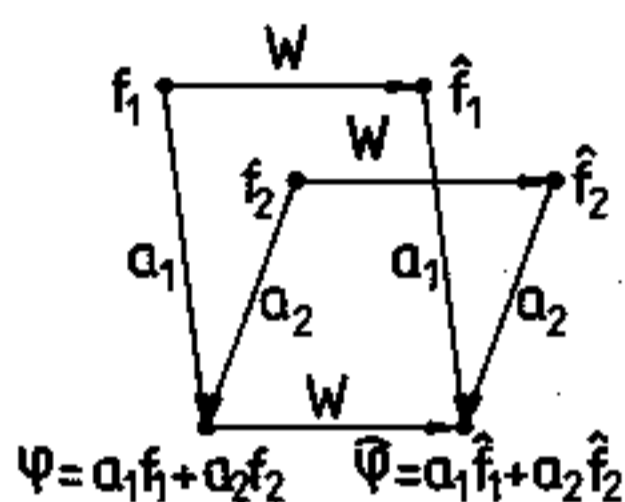
where $|V|$ is the number of elements in V .

spectral characteristic of switching functions, namely, the logical autocorrelation function B , which may be defined for the given system f of switching functions as

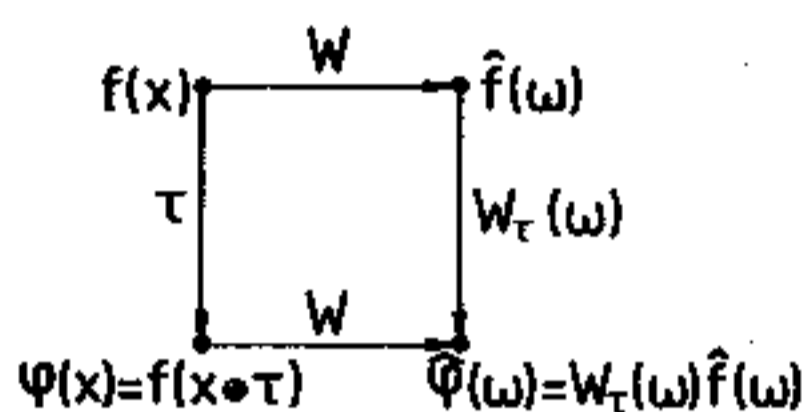
$$B(\tau) = \sum_x f(x) f(x \oplus \tau) \quad (14)$$

The following important result, which is an analog of the well-known Wiener-Khinchin theorem in the theory of stochastic processes, shows the relation between the autocorrelation function and the Walsh transform

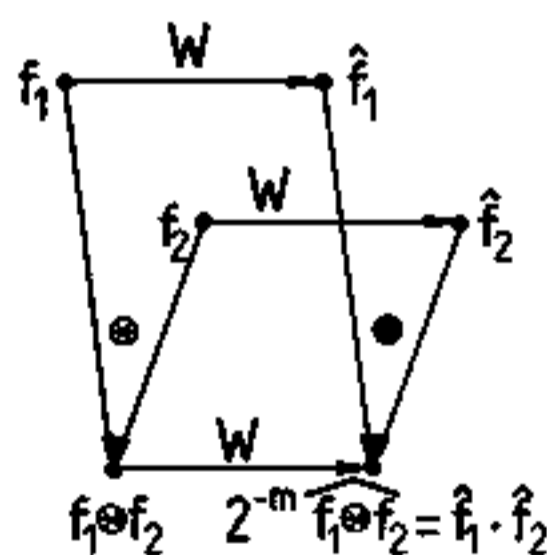
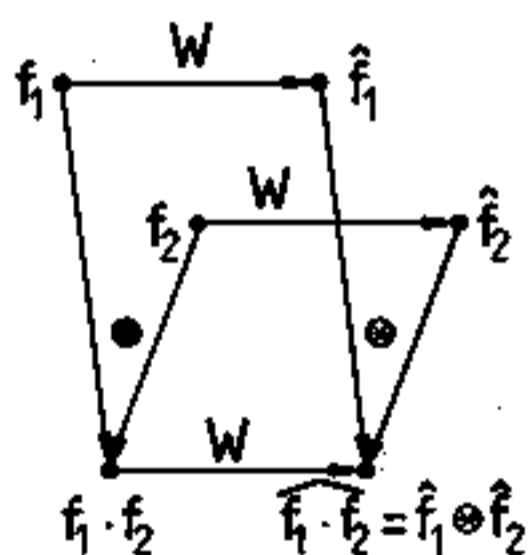
$$B = 2^{2m} \hat{f}^2 \quad (15)$$



a) Linearity (8)

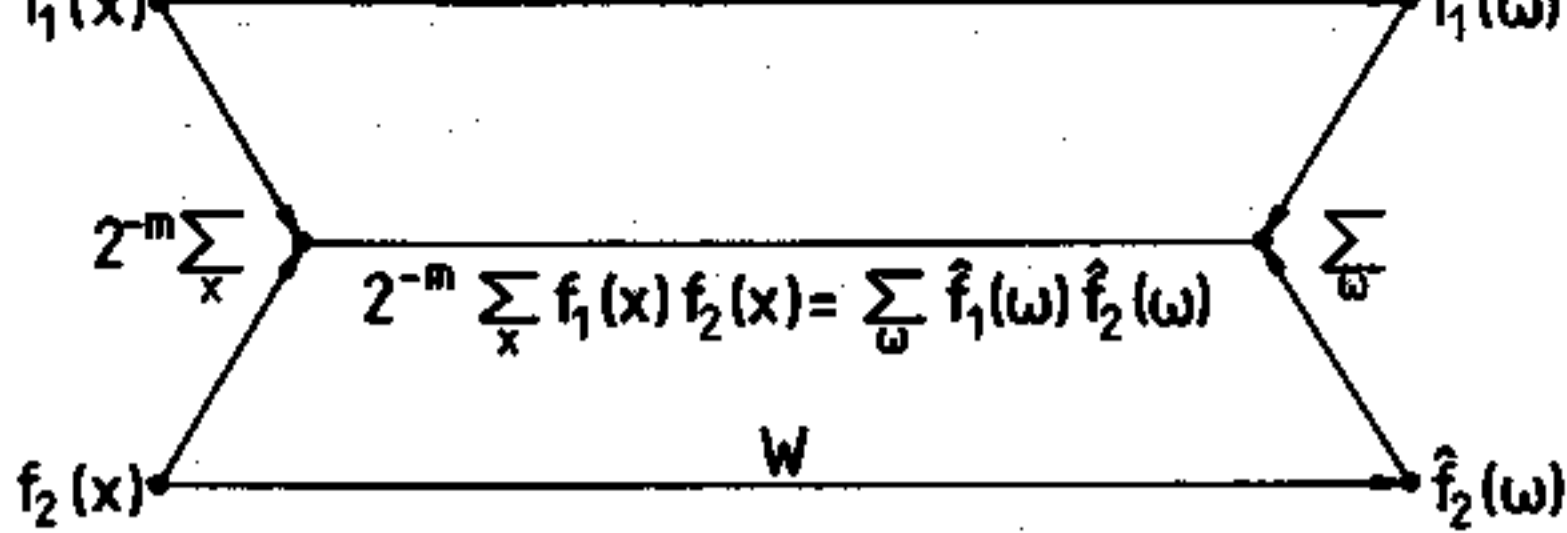


b) Translation of Arguments (9)

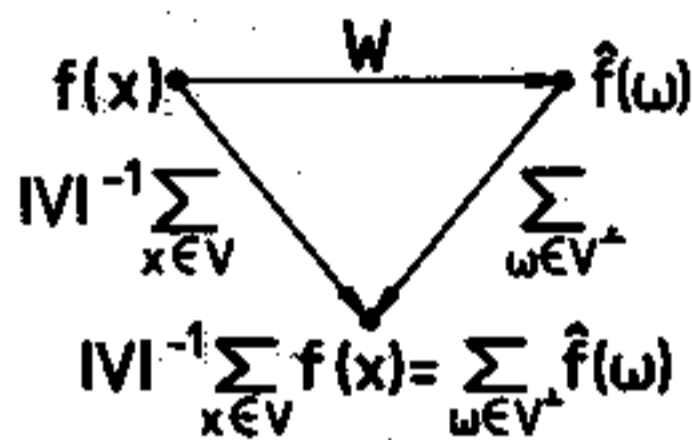


c) Logical Convolution (11)

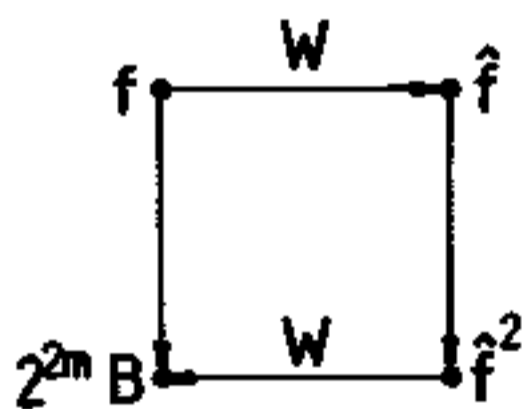
Fig. 2. Properties of the Walsh transform.



d) Plancherel Theorem (12)



e) Poisson Theorem (13)



f) Wiener-Khinchin Theorem (15)

Fig. 2. Properties of the Walsh transform (cont'd).

Successive application of the Walsh transform to the original function f . (Relations (8)–(15) are illustrated by Fig.2)

We note that the logical autocorrelation function is invariant under the dyadic shift (i.e., functions $f(x)$ and $f(x+t)$ have the same autocorrelation for any binary vector $t \in F_2^m$). The spectrum $\hat{f}(\omega)$ and the autocorrelation function $B(\tau)$ will be the most important analytical tools used in this book for spectral design techniques.

We also note that the basic properties (8) – (15) of the Walsh transform are very similar to the corresponding properties of the Laplace or the Fourier transforms, the major difference is the replacement of addition (or subtraction) by componentwise modulo 2 addition. To compute the Walsh transform $f(x) \rightarrow \hat{f}(\omega)$ we can use the Fast Walsh Transform algorithm [5,8,9,124]. For $\omega \in F_2^m$ this requires $m2^m$ additions and subtractions, and 2^m memory cells. This indicates that it is quite feasible to compute Walsh transforms and logical autocorrelations for systems of Boolean functions of, say, 20 arguments using modern computers. Tables of Walsh transforms and logical autocorrelations for different classes of Boolean functions may be found in [5].

The Walsh transform can be generalized to the case of non-binary (p -ary, $p > 2$) functions. This is relevant, for example, to image processing (see Chapter 3 and Chapter 5) and digital filtering (see Chapter 4). In this case Walsh functions $W_\omega(x)$ are replaced by the generalized Walsh (or Chrestenson) functions $X_\omega(x)$ where

$$X_\omega(x) = \exp \left(i \frac{2\pi}{p} \sum_{j=0}^{m-1} x_j \omega_j \right) \quad (i = \sqrt{-1}), \quad (16)$$

given that $x = \sum_{j=0}^{m-1} p^j x_j$, $\omega = \sum_{j=0}^{k-1} p^j \omega_j$, $x_j, \omega_j \in \{0, 1, \dots, p-1\}$.

defined at points $0, 1, \dots, N-1$ may be considered as a special case of the Chrestenson transform for $p=N$ and $m=1$.

All basic properties of the Walsh transform can be easily generalized to the case of the Chrestenson transform (see [5]). The Walsh transform is a special case of the Chrestenson transform for $p=2$.

The Chrestenson transform may be considered as a Fourier transform over the group F_p^m of all p -ary m -vectors (p not necessarily prime) with respect to the operations of componentwise modulo p addition.

To generalize the Walsh or the Chrestenson transforms to the case of an arbitrary commutative group G (e.g. when different components of vector x belong to the different alphabets, x_j , and the group operation in G is the componentwise addition, with components added modulo $|G_j|$, $j=0, \dots, m-1$) one should replace the Chrestenson functions (16) by the characters of the group G . Characters χ_ω are homomorphisms of G into the multiplicative group of roots of unity, i.e. for any $x, z \in G$ $\chi_\omega(x * z) = \chi_\omega(x) \chi_\omega(z)$ where $*$ is the operation in G and $|\chi_\omega(x)| = |\chi_\omega(z)| = 1$. Walsh functions and Chrestenson functions are characters of F_2^m and F_p^m correspondingly [5]. These generalized Fourier transforms may be further generalized to the case when G is a noncommutative group (for example, when $x \in G$ is a permutation of input terminals). In this case characters should be replaced by unitary irreducible representations of G , which are matrix-valued functions defined over the group G [10,11]. Generalized Fourier transforms over arbitrary finite commutative and non-commutative groups will be used in Chapter 3 and Chapter

In conclusion, we again note that all the basic properties of the Walsh transform (8)-(15), including the Fast Walsh transform algorithm, may be generalized to the Fourier transform over any finite group G [11]. Generalizations of the Walsh and

oids. These are known as the Walsh-Galois and the Chrestenson-Galois transforms [5,10,12].

The Walsh transform and its generalizations have been widely used in the analysis and design of digital devices. We will present below a very brief summary of these applications.

The earliest applications of the Walsh transform have been in the areas of Boolean function classifications, design techniques for logical devices and data transmission.

Spectral approaches for Boolean function classifications have been presented in [13, 14, 15, 19] and for the design of digital devices in [5,14 - 21,113,120]. Applications of the Walsh transform for data transmission started with the pioneering work of Harmuth [22] and continued in [23 - 26,38]. Spectral techniques have been also widely used in the theory of error-correcting codes and in particular for the proof of MacWilliams identities [27]. In addition, they have been useful to compute weight distributions of linear codes [28] and their subsets [29].

The Chrestenson transform has been used in multiple-valued logic (especially ternary logic), for design of devices with many possible states [30 - 35,118,119], and in the theory of non-binary error-correcting codes [27 - 29].

Another area where the Walsh transform and Walsh-related transforms have been widely used is signal processing, especially image processing and pattern analysis [6, 36-43]. The Walsh transform and its generalizations have also been used for digital filtering, construction of suboptimal Wiener filters and analysis of tradeoffs between the statistical performance of a filter and its computational complexity [42, 43, 122, 123, 125].

Spectral techniques for testing of logical networks by verification of the coefficients in the spectrum or in the autocorrelation function have been developed in [51 - 54, 117]. The problem of constructing optimal data compression schemes by

ticularly useful for compressing test responses of logical networks [44, 45], of memories [50], and for testing numerical computations [46, 47, 48]. Spectral techniques for reliability analysis of logical networks has been presented in [58, 120].

In this book, Chapters 1 and 2 are devoted to applications of spectral techniques for logical design. Chapter 3 deals with applications of these techniques to pattern analysis, and Chapter 4 with applications to digital filtering. Computer architectures for spectral processing and pipelining of data by cellular arrays are presented in Chapter 5. Here the presentation is made with emphasis on signal and image processing and on generalized spectral estimation algorithms.

Chapters 6, 7, 8, and 9 focus a special attention on the problems of testing, fault detection and correction in computer hardware.

With the advent of LSI and VLSI technology the growing costs of test generation and application of is becoming a real bottleneck of the computer industry. The major reasons for this are poor controllabilities and observabilities of internal nodes of complex devices and limited numbers of output pins. The time and the cost of testing increases tremendously (in general, exponentially) with the growing complexity of the devices to be tested. In many cases, this cost is higher than the cost of development and manufacturing. 'The majority of direct labor time required to build an Apple III is straight test time... If the test and the rework time is added together, 72% of the process time is accounted for' [59]. We may also recognize that generating an optimal test for detecting single stuck-at faults is already an NP-hard problem (i.e., the number of steps in any test generation procedure grows exponentially with the increase of the number of gates in the device under test) [2,3].

networks is the choice of a fault model. The fault model may depend on the device's logical structure, its electrical configuration and the environment where this device is to be used. The following fault models have been widely used: single and multiple stuck-at faults [61, 62, 83, 87], intermittent (transient, or soft) faults [87, 57, 58, 110], single and multiple bridging (short-circuit) faults [83, 105-108], pattern sensitive faults for semiconductor memories [83, 109], and stuck-open faults for CMOS devices [111, 112]. Stuck-at faults, bridging faults and intermittent faults are presently the most popular fault models in use. The stuck-at fault model is used in chapters 6, 7 and 8 of this book, the bridging fault model in chapter 6, and the intermittent fault model in Chapter 9.

For testing of small and medium scale integration devices gate-level approaches have been widely used. In this case the input data for test generation consists of a gate-level description of a device under test and a gate-level description of a class of possible faults. These gate-level test generation procedures have been based on the ideas of path sensitization [83], Boolean difference [61] and the D-algorithm [62, 116]. The Boolean difference (derivative) $\partial f/\partial x_i$ with respect to x_i for the Boolean function $f(x_0, \dots, x_{m-1})$ is defined as

$$\begin{aligned} \partial f/\partial x_i (x_0, \dots, x_{i-1}, x_{i+1}, \dots, x_{m-1}) = \\ f(x_0, \dots, x_{i-1}, 0, x_{i+1}, \dots, x_{m-1}) \oplus \\ f(x_0, \dots, x_{i-1}, 1, x_{i+1}, \dots, x_{m-1}) . \end{aligned} \quad (17)$$

A single stuck-at-1 (stuck-at-0) fault at line x_i is detected by a test vector $t = (t_0, \dots, t_{m-1})$ iff, respectively,

$$\begin{aligned} t_i \partial f/\partial x_i (t_0, \dots, t_{i-1}, t_{i+1}, \dots, t_{m-1}) = 1 \\ (t_i \partial f/\partial x_i (t_0, \dots, t_{i-1}, t_{i+1}, \dots, t_{m-1}) = 1) . \end{aligned} \quad (18)$$

modifications, have been and still are very useful for small and medium size devices, this is especially true for devices where design for testability guidelines [63, 87, 115] have been implemented. With the transition to VLSI technology there is a growing demand to develop more efficient testing procedures. There are several reasons for this. First of all, for VLSI devices, a gate-level description of the device is very complex and may not be available at all (to individual users). Even if a gate-level description is available to a test designer, the cost of test generation, is in many cases, prohibitively high for VLSI devices. These considerations stimulated the development of a functional testing approach as a viable alternative to gate-level testing, especially in the case of microprocessor testing.

For functional testing, the input data for test generation consists of a functional description of the circuit and of a class of faults [64-68]. For the functional testing of a microprocessor, the functional description may be a register-transfer-level one, and typical functional faults may be replacements of an instruction by another one, replacements of an instruction by no instruction or two instructions, etc. [65,67,68].

Functional testing techniques have been successfully used for many years for testing of complex devices. Nevertheless, for these approaches, the cost of VLSI test generation is very high, especially when a broad spectrum of devices has to be tested. In addition, it is difficult to estimate the efficiency of a functional test. For example, the percentage of faults of a given class, say single stuck-at faults, which are detected by the test may be difficult to calculate. In many cases the only way to estimate this fault coverage for a functional test is to perform a computer simulation using a large set of faults. Fortunately, software packages for the simulation are very expensive, and lengthy CPU times may be required to run these

In view of these difficulties, there is a growing tendency in the VLSI environment to eliminate as much of test generation as possible. The following four approaches have been used to achieve this goal:

1. universal standard tests for various classes of faults,
2. exhaustive or random testing, in combination with various data compression schemes, for the generation of test data and compression of test responses,
3. design for testability,
4. built-in self-testing approaches based on introducing redundancy into a device in order to provide self-error-detecting/correcting capabilities.

These approaches are considered in Chapters 6, 7, 8 and 9 of this book.

Fortunately, the same factors that make the problem of test generation for VLSI devices so difficult, namely, the increasing complexity and large diversity of the circuits, facilitate another approach known as universal testing [69-72]. Based upon probabilistic considerations, universal tests are designed to detect all faults of a given class in almost all devices. The fraction of devices in which universal tests detect all the faults of a given class, approaches one rapidly as the number of input lines for the circuit under test grows. For all practical purposes, this fraction can be put equal to one for the number of input lines $n \geq 20$. The transition from functional to universal testing is similar in principle to the transition from mechanics to statistical mechanics. The major breakthrough in communication engineering due to Shannon's information theory was based on very similar ideas.

The universal testing approach is presented in Chapter 6. For this approach, one does not try to develop a test for a specific device, but rather to construct a deterministic standard test that can then be used for a large set of devices. Note that

techniques suggested in [75 - 78] may be considered as special cases of universal testing. The universal testing approach further aimed to fill the gap between functional and random testing and to combine some advantages of both. For universal testing, the input data for test generation consists of parameters of the device under test (e.g., numbers of input and output lines, flip-flops, etc.) and a description of a class of possible faults (e.g., stuck-at faults of a given multiplicity). Generally speaking, universal tests require less test patterns than random tests but more than functional ones.

There are some similarities between random and universal testing, for instance, both approaches ignore the specific features of the device under test. Nevertheless, there are essential differences between these approaches that lead to different test sizes and fault detecting capabilities, and therefore these similarities may be misleading. First, universal tests are designed in a deterministic manner, where not only the test patterns but also their sequential order may be essential. On the other hand, the generation and application of random test patterns are intrinsically stochastic. Second, we note that in contrast with random testing, universal tests are fault oriented: they are designed for a specific class of faults.

Universal tests are efficient when a broad spectrum of complex VLSI devices should be tested, and a small probability of not detecting all the errors of a given class can be tolerated.

Chapter 6 presents universal tests and the corresponding capabilities of fault detection for single and multiple stuck-at bridging faults at input/output lines and faults in flip-flops. A detailed comparative analysis of universal vs. functional and universal vs. random testing is also presented in Chapter 6.

Another approach to testing that does not require a complex test generation procedure is that of random or exhaustive

millions of test patterns. In order to efficiently monitor test responses it is necessary to compress the output streams. The compression of an output sequence of, say, 10^6 bits may result in a 16-bit signature that is to be monitored for fault detection or fault location. The optimal choice of a data compressor for a given class of errors is very difficult to refine. In addition, the probability of masking an error by a given data compressor must be estimated. (Note that we mean by error a manifestation of a fault at the output of a device under test.)

Chapter 7 presents spectral techniques for data compression. These techniques are based on verification of some precomputed spectral coefficients $\hat{f}(\omega)$, where \hat{f} is the Walsh transform of a system of Boolean functions, f , describing the behavior of the fault-free device.

Another approach to the compression of test data makes use of single or multiple input linear feedback shift registers (LFSR), which are shift registers with XOR gates in their feedback loops [79, 80]. For this approach, as well as for almost all other known data compression techniques, (like syndrome testing [73, 74], or transition counting [81, 82, 83]), data compressors are sequential devices implementing 'time compression' of an output data stream.

A different approach to the same problem is based on the idea of 'space compression' [84, 121]. In this case the data compressor is a combinational device with a smaller number of output lines than that in the device under test. Only output lines of the 'space compressor' are monitored for testing. The theories of 'space data compression' [84] and 'time data compression' [79, 80, 84, 121] are related to the theories of linear error-correcting codes and cyclic error-correcting codes, respectively. The best 'space' or 'time' data compressors for the given class of errors correspond to decoders of optimal

A survey of data compression techniques useful for fault detection and fault location (diagnosis) is presented in Chapter 7. A special attention in this chapter is devoted to linear feedback shift registers (LFSRs), since at the present time these are the most popular tools for compressing test responses. Most all results published in this area are devoted to applications of LFSRs for fault detection. A survey of these results and new results on fault diagnosis by LFSRs are presented in Chapter 8.

Since testing remains very expensive while the cost of hardware is decreasing, there is a growing interest in using built-in on-line concurrent self-tests. In this case, working testing modes are combined, and a redundancy is introduced to provide self-error-detecting and/or self-error-correcting capabilities. A built-in self-test may be efficiently used for detecting not only stuck-at faults but intermittent faults as well. (Note that gate-level, functional, random and universal testing approaches, as described above, are not efficient for detecting intermittent faults.) On the other hand, it is very difficult to test networks with built-in fault correction. The following techniques have been considered for self-error-detection and correction: replication, 'interwoven logic', and parity or correcting codes.

For replication techniques several copies of a device are used, and outputs of these copies are compared for fault detection [85-87], or a special threshold element ('voter') is used to correct, (or 'mask') errors [87-88]. Note that voters themselves may also be replicated [87]. Different configurations, self-purging replication and adaptive voting techniques have been suggested [87, 113, 114]. When a faulty copy is identified by comparing its output with the output of the voter, the faulty copy is automatically switched out and a spare copy switched in. In spite of the fact that replication

military and civil applications, especially in the form of replication and triplication.

Another set of well-known approaches for self-error-correction, is referred to as 'interwoven logic' [89 -93]. Here we are trying to construct a network in such a way that the gates at any given level in the network will mask a maximal number of errors that appear in the gates and lines of the previous level. This approach results in redundant inputs to each gate to provide for gate-level fault-masking. A major disadvantage of the 'interwoven logic' is that its implementation results in very high redundancy, which may even decrease the reliability of the whole system.

In view of all this, there is a growing interest in the application of error-detecting and error-correcting codes for the design of reliable devices. The simplest form of these techniques is parity checking. We also note that replication techniques may be considered as a special case of the application of error-correcting codes. (These are called 'repetition codes', with a small transmission rate, but a very simple decoding procedure [87]). Techniques for a reliable design based on error-detecting and error-correcting codes may be efficiently used for designing control sections of computers. The behavior of a control section may be described by the finite automaton (sequential machine) model. Here, error-detecting and error-correcting codes may be used for the finite automaton's state assignment or for a reliable implementation of the corresponding sequential network's combinational part. In the latter case we add a few input and output lines for every logical subnetwork. This is done in such a way that input and output vectors of the fault-free subnetwork are codewords of the chosen code [87, 96 - 104]. This approach is promising since it results in high-speed logical networks with distributed error detection or correction. Chapter 9 provides further details for this approach.

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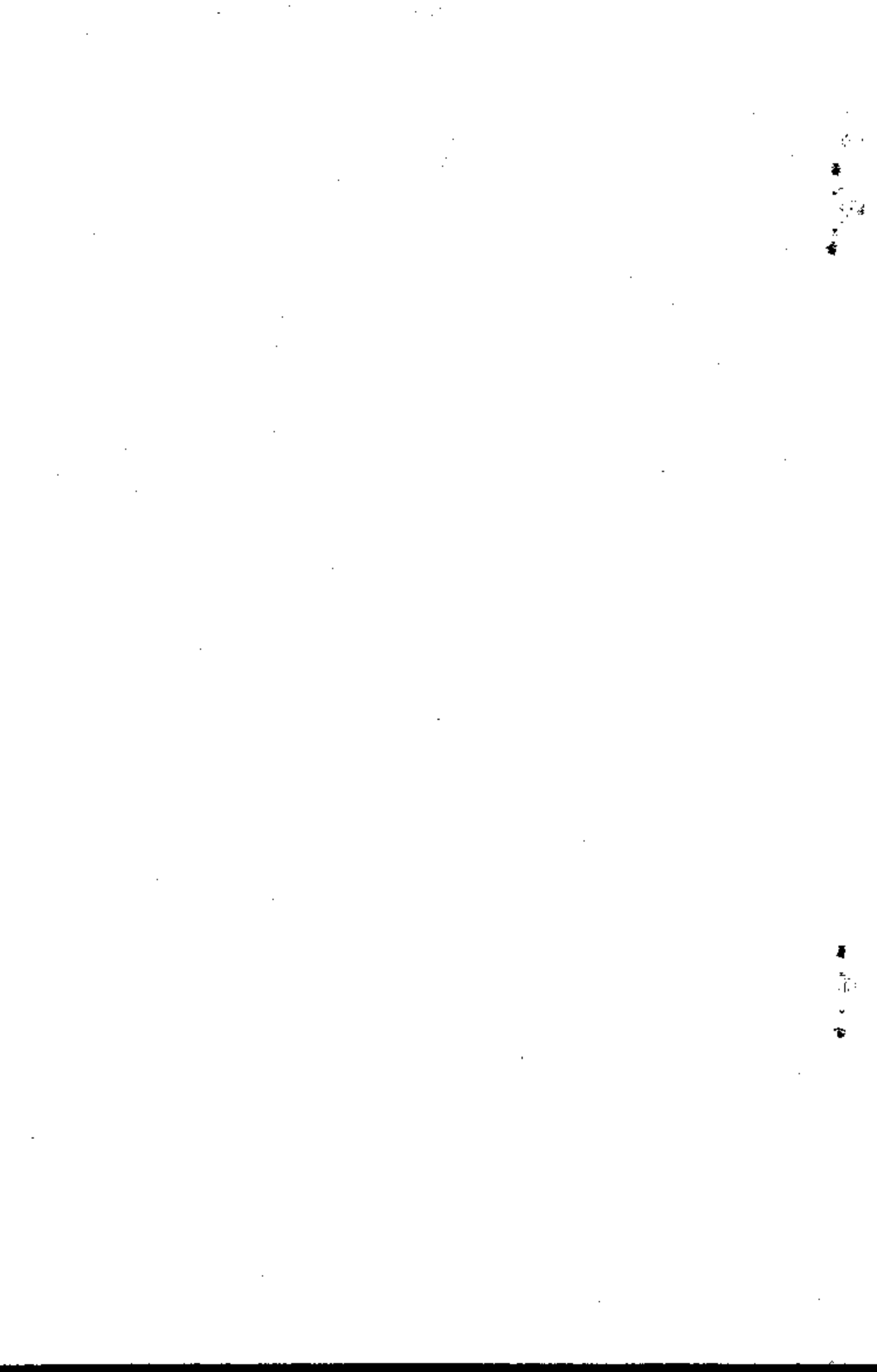
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Department of Electrical, Computer and
Systems Engineering
Boston University
Boston, MA, USA

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