Hard and Soft Decisions in Diagnosis by Space-Time Signatures

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Abstract

We propose a new approach for identification of faulty processing elements in computing arrays based on the compressed response of the system. The test response is compressed first in space and then and faulty processing elements are identified by "hard decision decoding' of the corresponding space-time signature. The approach results in considerable savings in hardware required for diagnostics. There exists a remarkable similarity between the problem of finding the optimal matrix for the time compression and that of constructing the check matrix of the best code that corrects a given set of error patterns. The major difference, however, is that the operations over GF(2) should be replaced by Boolean operations. An alternative approach of "soft decision" signature decoding is discussed.

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Summary

Let us consider the diagnosis problem for a system of (not necessarily identical) processing elements (e.g., a systolic array). The system is represented by a directed graph G whose nodes correspond to Processing Elements (PEs) and directed edges correspond to communication links. Our approach to the diagnosis problem is based on signature analysis of test responses. Signature analysis has been widely used for chip and board level testing and diagnosis [1–12].

Consider first the straightforward approach to diagnosis signature analysis. Test responses $y(t)=(y_1(t),...,y_n(t))$ at the moment t ($y_i(t)$ is a b-bit binary vector) are transferred via the system bus into a redundant chip in such a way that the test response $y_i(t)$ at the output i is compressed in time by Linear Feedback Shift Register (LFSR) i. After all test responses y(1),...,y(T) (T is a number of test patterns) have been compressed by the LFSRs, the corresponding signatures $s_1,...,s_n$ are compared with the precomputed reference signatures $s_1,...,s_n$ and the error vector $\mathbf{e}=(\mathbf{e}_1,...,\mathbf{e}_n)$ is computed, where $\mathbf{e}_i=1$ iff $\mathbf{s}_i\neq\mathbf{s}_i^0$, and $\mathbf{e}_i=0$ otherwise. The identification of a faulty PE is implemented by the $\mathbf{n}\times\mathbf{N}$ decoder (\mathbf{N} is the total number of PEs in the system) with the input $\mathbf{e}=(\mathbf{e}_1,...,\mathbf{e}_n)$.

We assume that a number of test patterns T is sufficiently large, so that a fault in a PE will manifest itself by distortions of signatures corresponding to all output PEs connected with the faulty PE. The probability of masking is very small for large b [1, 7–9].

The system is diagnosable iff all n-bit error vectors are different and not equal to (0,...,0).

An important practical case is when at most one PE or any number of incoming links to this PE may be faulty. Then, the obvious lower bound on the number of outputs n of a diagnosable system is $n \ge \lfloor \log_2(N+1) \rfloor$, where N is the total number of PEs in the system.

For the straightforward approach to diagnostics the required hardware overhead L_1 , in terms of the number of equivalent two-input gates, is of the order of L_1 =O(bn)+O(Nn). For example, for the eight-level binary tree with b=32 we have n=128, N=255 and L_1 ≈110,000 (assuming that one flipflop is equivalent to 8 gates).

In this paper another approach to diagnostics is described which results in a considerable reduction of the required overhead while the probability of missing a fault remains small. It is shown that in many cases the overhead can be decreased to $L_2=O(b\log_2 n)+(N\log_2 n)$. This approach does not require redesigning and introducing selftest into PEs. Fault location in this case is implemented by a standard additional PE which generates test patterns, compresses responses (signatures) to identify faulty PEs. The structure of this additional PE does not depend on the structures of PEs in the original system.

In general, the proposed approach can be described as follows. The output response vector $y(t)=(y_1(t),...,y_n(t))$ is compressed in space into $z(t))=(z_1(t),...,z_r(t))$ where $y_i(t)$ and $z_i(t)$ are binary vectors, z(t)=Hy(t) and $z_i(t)$ and $z_i(t)$ are binary vectors, $z_i(t)=Hy(t)$ and $z_i(t)$ and $z_i(t)$ are binary vectors, $z_i(t)=Hy(t)$ and $z_i(t)$ and $z_i(t)$ are signature of output vectors for this counter is the sequence of $z_i(t)$ are compressed in time by $z_i(t)$. Final space—time signatures $z_i(t)=(z_1(t),...,z_r(t))$ are compressed in time by $z_i(t)$ and the resulting

error syndrome $e^c = (e^c_1, ..., e^c_r)$ ($e^c_i = 1$ iff $s_i \neq s^0_i$) is decoded to indicate the faulty PE. This identification is possible iff there is a one–to–one mapping between PEs and error vectors $e^c = (e^c_1, ..., e^c_r)$ ($e^c_i \in \{0,1\}$). This mapping $e^c(i)$ (i=1,...,N) defines an embedding of the graph G representing original system of PEs into the r–dimensional binary cube. The set of vertices of the r–dimensional binary cube (i.e. the set of all r–bit binary vectors) is a partially ordered set: we consider vector a to be a descendant of vector b, if a can be obtained from b by replacing some of the components equal to 1 by zeros. (It is said also that b covers a). The embedding of graph G into the r–dimensional cube must preserve the partial ordering on G defined by its directed edges, i.e. if (i,j) and (i,q) are directed edges in G, then $e^c(i) = e^c(j) \vee e^c(q)$.

An overhead for the space-time compression is of the order of L_2 =O(br)+O(Nr), and comparing with the overhead L_1 for the straightforward approach we have

$$\frac{L_1}{L_2} \cong \frac{n}{r}. \tag{1}$$

Since $r \le n$ the space—time compression technique is more efficient than the straightforward approach. To minimize the overhead one has to minimize the length r of syndromes e^c . Since all error syndromes must be different and not equal to (0,...,0) we have the following (attainable) bounds

$$\lceil \log_2(N+1) \rceil \le r \le n. \tag{2}$$

The overhead minimization problem for the space—time signature diagnostics can be reduced to constructing an $(r\times n)$ matrix H with minimal r such that the system remains diagnosable after the space compression z(t)=Hy(t) of its output y(t).

It is shown, that the relation between the error vectors e in the original system and error syndromes e^c is given by the following formula:

$$e^{c}=H\otimes e$$
 (3)

where \otimes stands for the Boolean multiplication of an $(r \times n)$ binary matrix by an n-bit binary vector e with addition being replaced by OR. Thus, the overhead minimization

problem can be formulated in the following way: construct a space compression matrix H with a minimal number of rows such that for any two error vectors e and e'

$$H \otimes e \neq H \otimes e'$$
, $H \otimes e \neq 0$, $H \otimes e' \neq 0$. (4)

The set of error vectors e is defined by the topology of interconnections in the original system, and the number of error vectors is equal to N.

It is remarkable that condition (4) on matrix H is similar to the necessary and sufficient condition for the check matrix of a code correcting error patterns defined by the graph G. The major difference, however, is that in our case operations over GF(2) is replaced by Boolean operations.

This paper considers the minimization problem of the overhead for several important classes of systems: balanced binary and p-ary (p>2) trees, 2-dim rhombic meshes, triangular meshes and cubic meshes. These arrays have been widely used [14,15]. Close lower bounds on r are obtained for specific classes of arrays, and nearly optimal constructions for space compression matrices. H are given. The results show that space-time signature diagnostics provides substantial hardware savings as compared to the straightforward approach (time compression only). For example, for a rhombic array with N=864, n=108 and b=32, the straightforward approach requires approximately L_1 =10⁵ equivalent two-input gates, while the suggested method requires only L_2 =1.2·10⁴ gates. For a binary tree with N=255 and b=32, L_1 =110,000 and L_2 =10,000.

The space—time diagnostic approach described above can be applied to location of multiple faults in arrays of PEs. To locate a fault with multiplicity 1 (I PEs are faulty) we use an l—step sequential procedure. At every step we run the space—time diagnostic procedure described above, identify one faulty PE, replace it and then repeat the procedure again. We show that using the same hardware required for location of single faults one can locate a considerable portion of multiple faults by the multistep sequential error location.

The proposed space—time signature approach to diagnostics is based on the "hard decision" decoding of signatures $s=(s_1,...,s_r)$, when we can identify a faulty PE by analyzing binary vector e^c which indicates the distorted component in s. The magnitudes of distortions are not important for the hard decision procedure. An alternative approach is

the "soft decision decoding" of $s=(s_1,...,s_r)$ for the space—time signature diagnosis. In this case the identification of a faulty PE is based on the analysis of magnitudes of distortions in components of s. Soft decision techniques have been developed in [11,12] for board—level space—time signature diagnosis and in [13] for space—time diagnosis of multiprocessor systems. In [11,12] and [13], the assumption has been made that components of the system are disconnected in the testing mode. In this paper we consider both hard and soft decision prosedures under the assumption that, in the testing mode, components of the system—under—test are interconnected in the same way as in the computing mode.

References

- [1] Smith J. E., "Measures of the Effectiveness of Fault Signature Analysis" IEEE Trans. on Computers, 1980, c-29, pp510-516
- [2] McAnney W. H. and Savir J., "There is Information in Faulty Signatures", Proc 1987 Int. Test Conference, Sept 1987, pp 630-636
- [3] Savir J. and McAnny W. H., "Identification of Failing Test with Cyclic Registers," Proc 1988 Int. Test Conference, Sept 1988, pp 322-328
- [4] Konemann B, Mucha J and G. Zwieholf, "Built-in Test for Complex Digital Integrated Circuits", IEEE J. Solid State Circuits, Vol SC-15 No 3, June 1980, pp 315-318
- [5] Upadhyaya S. J. and Saluja K. K., "Signature Techniques in Fault Detection" in "Spectral Techniques and Fault Detection", M. Karpovsky editor, Academic Press, 1985, pp 421-477
- [6] Bardell P. H. and McAnney W. H., "Self-Testing of Multichip Logic Modules", Proc. Int. Test Conference 1982, pp 200-204
- [7] Williams T. W., Daehn W., Gruetzner M. and Starke C. W., "Bounds and Analysis of Aliasing Errors in Linear Feedback Shift Registers", IEEE Trans. Computer-Aided Design, Vol 7, Jan 1988, pp 75-83
- [8] Ivanov A. and Agarwal V. K., "An Analysis of the Probabilistic Behavior of Linear Feedback Shift Registers", IEEE Trans. Computer-Aided Design, Vol S, No 10, Oct 1989, pp 1074-1088
- [9] Pradhan D. K., Gupta S. K. and Karpovsky M. G., "Aliasing Probability for Multiple Input Signature Analyzer", IEEE Trans on Computers, April 1980
- [10] Reddy S. R., Suluja K. K. and Karpovsky M. G., "A Data Compression for Built-In Self Test", IEEE Trans. on Computers, Sept 1988, pp 1151-1156

- [11] Karpovsky M. G. and Nagvajara P., "Board Level Diagnosis", Proc. Int. Test Conference, 1988, pp 47-53
- [12] Karpovsky M. G. and Nagvajara P., "Design of Self-Diagnostic Boards by Signature Analysis", IEEE Trans. on Industrial Engineering, April 1989
- [13] Karpovsky M. G., "An Approach for Error Detection and Error Correction in Distributed Systems Computing Numerical Functions", IEEE Trans. on Computers, Dec 1981, No 12, pp 947-954
- [14] Hwang K., Briggs F. A., "Computer Architecture and Parallel Processing", Mc-Graw Hill, 1984
- [15] Kung S. Y., "VLSI Array Processors" in "Systolic Arrays", Adam Higler, 1987