Signature Testability of PLA

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Abstract. This paper deals with the design of a Built-In Self Test (BIST) environment for the Programmable Logic Arrays that minimizes the aliasing probability. The signature testability condition is developed that prove criteria to compare the BIST environment aliasing. An important feature of the developed approach is that the criteria proved by signature testability allows to design both pseudo-random test pattern generator (PRPG) and signature analyzer (SA).

1 Introduction

The aliasing is an important problem in the compact technique. The aliasing occurs when the fault signature is identical to the fault-free one. The aliasing probability of the compact technique has been studied by coding theory framework [1]. In [2], the detection properties of the BIST environment for the errors that can be expressed as a single product term has been discussed. It has been shown that the BIST schemes based on the PRTG and the SA with the same feedback polynomial detect almost all cases of the above errors. Furthermore, the BIST environment with reciprocal polynomials have the poor error detection capability.

Here, we propose a signature testability condition that allows to determine the error detection capability for all combinations of PRTG- and SA-polynomials. We also propose a new error model generalized the one in [2]. The signature testability condition is derived to analyze the aliasing for proposed error model.

2 Signature Testability

Consider an algebraic model of a testing configuration that is shown in Fig. 1. Let $g(x)$ denote the primitive feedback polynomial of the PRTG and let $h(x)$ denote the irreducible feedback polynomial of SA. It is assumed that $deg\ g(x) = deg\ h(x) = m$. In this paper, α denotes the primitive element over $GF(2^m)$ defined by the primitive polynomial $g(x)$. The irreducible polynomial $h(x)$ defines the element β over $GF(2^m)$. Let $\beta = \alpha^k$. We assume here that the initial state of SA is zero. Initial state of PRTG is $0 \ldots 010$ and can be described by the element α. Let PRTG generate $2^m - 1$ test patterns, that are applied to the CUT.

Now consider the signature value for an Boolean function f that describes CUT. Let $f(\gamma)$ denote the value $f(g_{m-1}, \ldots, g_0)$ of the Boolean function f, where

$\gamma \in GF(2^m)$ and $\mathbf{G} = (g_{m-1}, \ldots, g_0)$ is the vector form of the element γ in the bases $1, \alpha^1, \ldots, \alpha^{m-1}$. Then [2],[3]

$$Sg(f) = \sum_{i=0}^{2^m-2} f(\alpha^i)\, \alpha^{-ik}. \tag{1}$$

In this paper, the criteria to estimate the aliasing of the BIST environment is discussed that based on the following error model.

Let $f(x)$ and $f_e(x)$ denote the Boolean function of the fault free and faulty CUT, respectively. The error function is given by $e(x) = f(x) + f_e(x)$, where $+$ denote the modulo two sum. We consider the Reed-Muller canonical form of the error function that is the modulo two sum of the terms. Let r be the literals number in the term with the maximum multiplicity.

Let the fault be called a signature testable fault if

$$Sg(e) = \sum_{i=0}^{2^m-2} e(\alpha^i)\, \alpha^{-ik} \neq 0. \tag{2}$$

Let us consider a set F of Boolean functions that have no more then r literals in the term with maximum multiplicity. For each function $f \in F$ the following vector can be formed: $v[f] = [f(\alpha^{2^m-2}), f(\alpha^{2^m-3}), \cdots, f(\alpha^0)]$. The set of vectors forms a vector subspace over $GF(2)$. This vector subspace is the r-th order Reed-Muller code $R(r, m)$ [4]. For each vector $v[f]$ can be formed polynomial $P(f) = \sum_{i=0}^{2^m-2} f(\alpha^i)x^i$. Common to all polynomials roots form a set of code nulls. The nulls of the rth-order Reed-Muller code have the following property.

The α^k is a root of the generator polynomial of the rth-order Reed-Muller code $R(r, m)$ if and only if $0 < w_2(k) < m - r$, where $w_2(k)$ is the binary weight of integer k [4].

Let error multiplicity be r. Then, the error sequence belongs to the rth-order Reed-Muller code $R(r, m)$. The set of the nulls of the code corresponds to a set of the SA for that the code word is an error causes the fault masking. Thus, the error with the multiplicity r is undetectable for all SA that have the feedback polynomial with root $\beta = \alpha^k$ and $m - w_2(-k) > r$.

Let $\sigma[g, h] = m - w_2(-\log_\alpha \beta)$, where α, β are roots of $g(x)$ and $h(x)$, respectively.

Signature testability condition. *The error with multiplicity r is signature testable if $\sigma[g, h] \leq r$.*

Hence, the BIST environment has the good error detectability when $\sigma[g, h]$ is small. The PRTG-SA pair has the minimum aliasing if $\sigma[g, h] = 1$. That is when $g(x) = h(x)$. The worst error detectability is when $\sigma[g, h] = m - 1$. The feedback polynomials of PRTG and SA are reciprocal in this case.

Now, we apply the signature testability condition to design the BIST environment. Let us analyzed the circuit error distribution over the error multiplicity r. We assume that in the digital circuit the errors with multiplicity $r > \rho$ occure only. Thus, feedback polynomials with $\sigma[g, h] \leq \rho$ must be used.

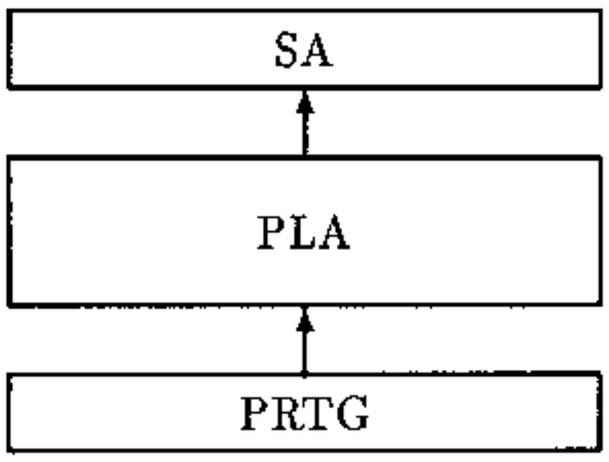

Fig. 1. Testing Configuration

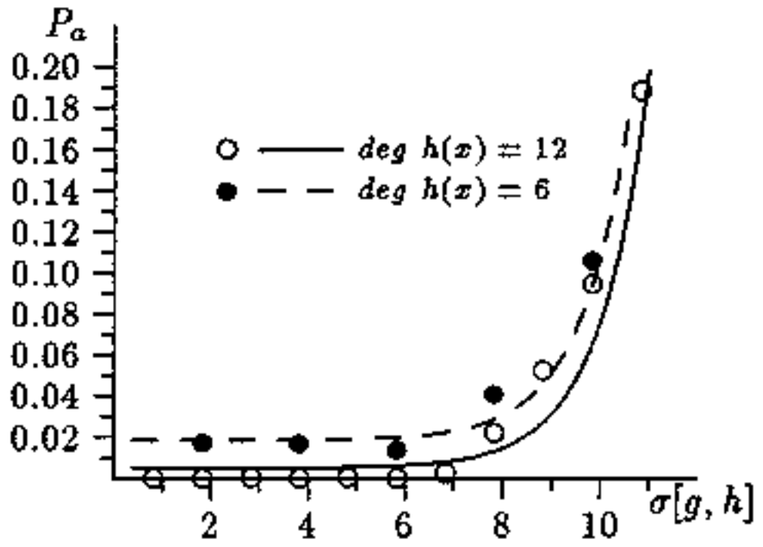

Fig. 2. Aliasing probability of BIST

3 Experimental Results

Some simulation experiments were performed to test the signature testability condition. Fig. 2 presents the results of one such experiment. The simulation experiments were done on the (12,103,12)-PLA. The aliasing probability was calculated for all cross-point-faults. The plot shows that primitive polynomials of the same degree can have the significantly different aliasing. The obtained σ-dependence of the aliasing probability supports the signature testability condition proposed. The experimental results show that the BIST environment with the $\sigma[g,h]$value close to m have the low error detection capability. The feedback polynomial $h'(x)$ of the 6 degree can have the lower aliasing than the 12-polynomial $h''(x)$ when $\sigma[g,h'] > \sigma[g,h'']$.

4 Conclusion

In this paper, the signature testability technique is developed that can be used to analyze aliasing of the BIST environment for Programmable Logic Arrays. The proposed approach is a first technique to estimate aliasing of both PRTG and SA, what have not been available yet.

The group of the BIST environment with the good error detection capability can be obtained by the signature testability condition. By using the property of the error distribution and the testability condition, the design procedure for BIST environment is proposed.

References

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