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The authors present an analysis and design of a pseudorandom pattern generator (PRPG) for boundary scan design chips with built-in self-test (BIST) where an s-stage PRPG is used for generating T distinct r-bit test patterns (in general, s * r). A method of connecting the PRPG outputs and the primary inputs of the chip-under-test that ensures a one-to-one correspondence between the state transitions of the PRPG and the r-bit test patterns is given. For the case when $r \geq s$, $T \leq 2^s - 1$ distinct r-bit test patterns are produced within T clock pulses. For the case when $r < s$, an estimate on the average number of clock pulses $\bar{N}(s, 2^r, T)$, (assuming randomly chosen initial states for the PRPGs), required for generating $T \leq 2^r$ distinct r-bit test patterns is derived and shown to be very close to the experimental values. This estimate can be used as a benchmark for selecting parameters and initial states of PRPGs for the case $r < s$.

PSEUDORANDOM TEST PATTERNS GENERATION FOR BUILT-IN SELF-TEST BOUNDARY SCAN DESIGN

The traditional board-level testing basically consists of testing of individual chips by use of bed-of-nail probes (in-circuit test), then testing of the interconnects between the chips, and, finally, the function of the entire board.[1] With the trends towards surface-mount boards and miniturization of printed circuit boards in-circuit test is no longer a simpe task and consequently becomes costly or even impossible.

In contrast with this, the use of boundary-scan technique in the design-for-testability of printed circuit boards is rapidly becoming an industry standard. In boundary-scan design chips, shift-register latches are placed adjacent to each pin and can be reconfigured in the test mode as a shift register providing a means for controlling and observing signal at the chip boundary by scanning in and out the test data via the test-data-in (TDI) and test-data-out (TDO) ports. Further, these boundary-scan chips are serially connected by the scan path in which the test data can be scanned in and out, and, thus, testing of chips and their interconnection are done via the board-edge connector.

The Joint Test Action Group (JTAG) together with the IEEE working group P1149.1 has proposed the boundary-scan architecture standard[1] to conform the implementation of boundary-scan design of the integrated circuits produced by different manufacturers. The proposed archictecture with four additional pins, a ready-to-implement hardware design (registers, multiplexers and the control unit) and the functional modes are given and defined in that document.[1] Recent works on the testing of the control unit (called the Test Access Port Controller) and on the testing and diagnostics of the

interconnects between chips designed based on JTAG/IEEE P1149.1 Standard can be found in [2] and [3], repectively.

BUILT-IN SELF-TEST BOUNDARY SCAN DESIGN

Built-in self-test (BIST) design of a board can either be approached by inclusion of an additional chip performing the test generation, signature analysis and diagnosis of the faulty chip[4] or by inclusion of a BIST facility in each chip on the board. The latter approarch was considered in [5] and [6] where several problems related to estimation of test generation time have ben formulaed. These problems are reviewed and solved in the present article.

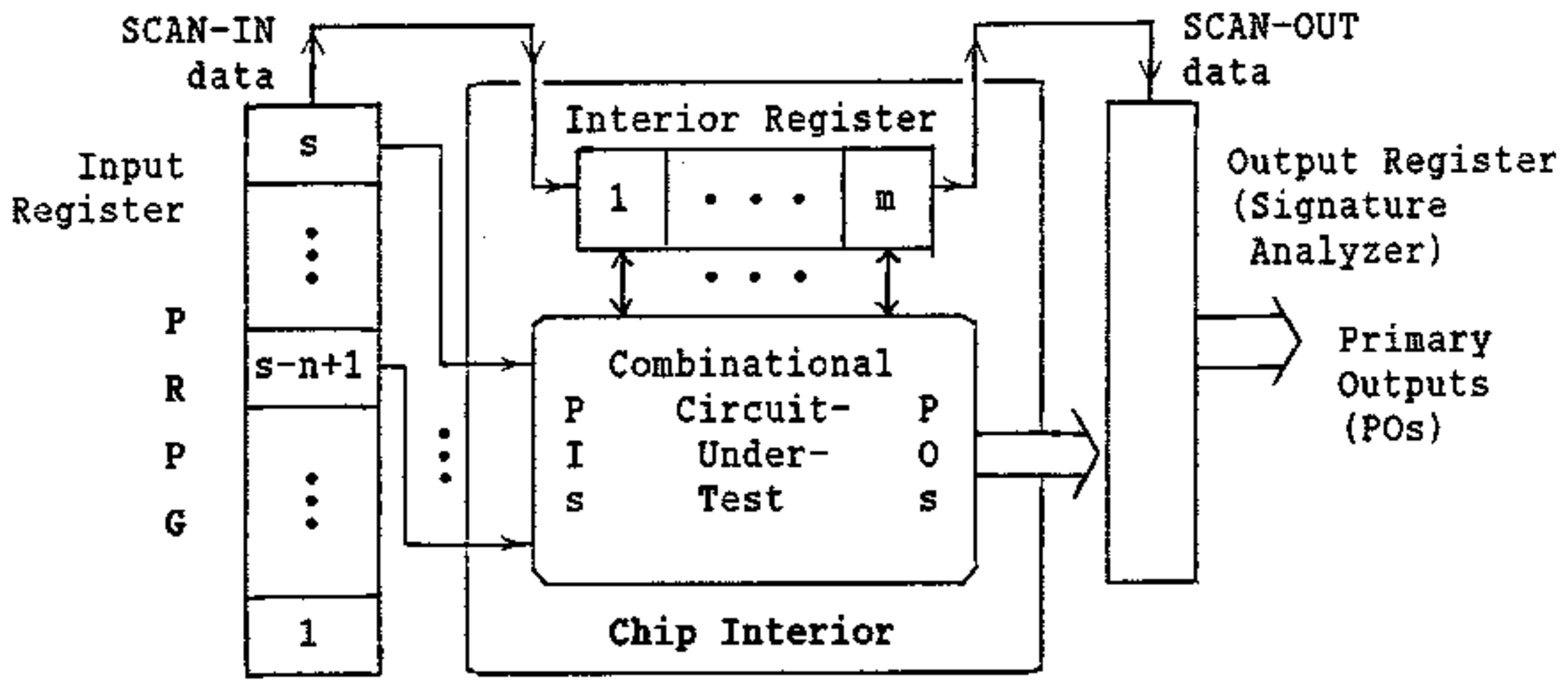

Fig. 1. Built-in Self-test Boundary Scan Template (Test pins not shown)

Boundary-scan-design templates[5] with BIST have been proposed as standard cells compiled in a VLSI design CAD tool. For these templates, the test procedure in the BIST mode can be described as follows. The input register is configured to function as a pseudorandom test pattern generator (PRPG). The PRPG is implemented by a maximal-length-sequence linear sequential circuit,[7,8,9] capable of generating 2^s-1 different nonzero s-bit patterns where s is the number of flip-flops in the PRPG. A test pattern at any moment consists of r = n+m bits where first leftmost bits are the contents

of n flips-flops of he PRPG connected to the primary inputs (PIs) of the chip interior and the next m consecutive bits are obtained by scanning-in the content of the last PRPG flip-flop to an m-bit interior scan register via the scan-in data path, (Fig. 1). Once an r-bit test pattern is applied to the chip-under-test the response at the primary outputs is latched into the output register which is configured to function as a multiple-input signature analyzer. At the same moment the m-bit next state response is latched back into the interior register. At the next clock pulse this response becomes the content of the interior register. The next state response is shifted out from the interior register to the signature analyzer and simultaneously the new m-bits test pattern generated by the PRPG is shifted into the interior register. After this a new test cycle begins. Finally, when the desired number of T distinct r-bit test patterns have been applied to the chip-under-test the signature produced by the output register is scanned out, observed at the board-edge connector and compared with the reference.

EFFICIENT TEST GENERATION FOR BIST BOUNDARY SCAN DESIGN

The first problem involved in the test generation for the BIST procedure described is that a design where the connections from the PRPG to the primary inputs (PIs) of the chip-under-test are chosen arbitrarily (e.g. from the first n cells of the PRPG as originally suggested[5,6]) does not provide for a full pattern coverage, that is, when $r \geq s$ the r-bit patterns obtained may not all be distinct.

We show that, for the case when $r \geq s$ ($r = n+m$), 2^s-1 distinct r-bit test patterns can be generated by shifting the PRPG at most $s-n+2^s-1$ times, provided that the contents of the last n consecutive cells of the PRPG are the test patterns applied to PIs and the content of the rightmost cell is

scanned into the interior scan register. Examples of the proposed connections are given in Fig 2, 3 and 4, for different implementations of the PRPGs.

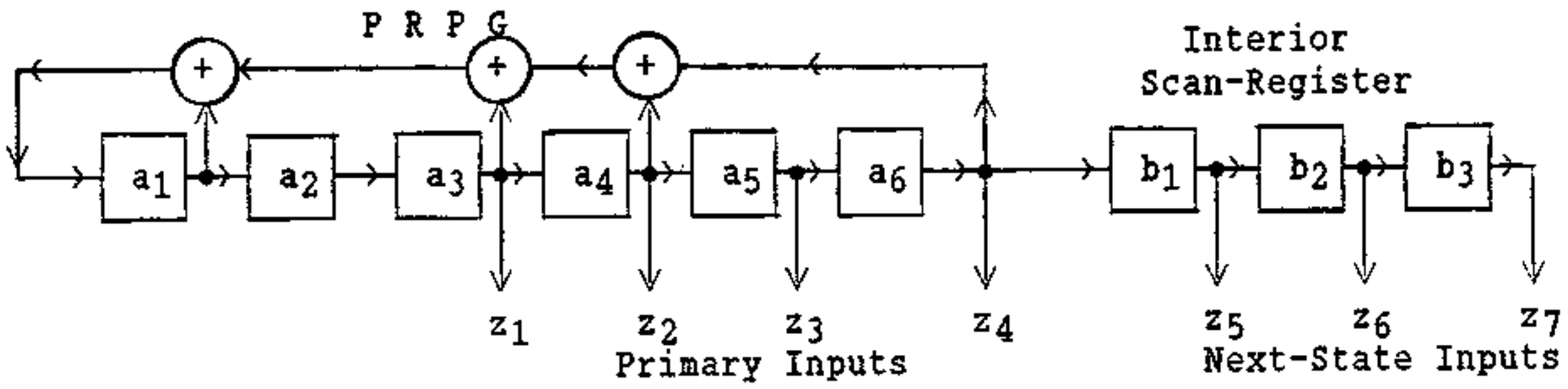

Fig. 2. An example of Efficient Test Generation: (s,n,m)=(6,4,3), r=n+m=7, with External XOR-Gate LFSR Realization of the PRPG, (The Characteristic Polynomial, $f(x) = x^6 \oplus x^5 \oplus x^3 \oplus x^2 \oplus 1$).

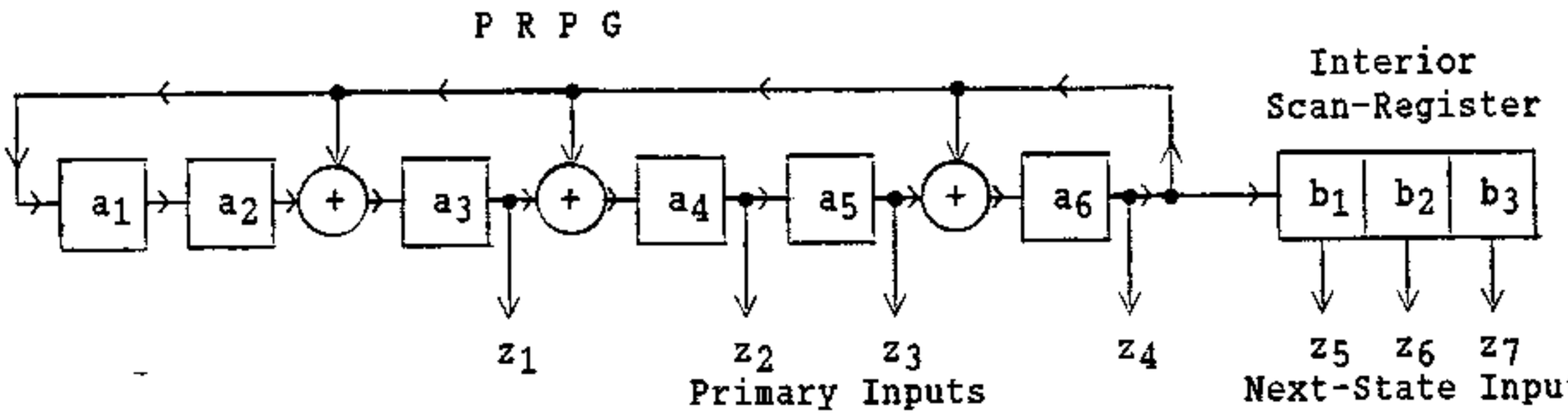

Fig. 3. An example of Efficient Test Generation: (s,n,m)=(6,4,3), r=n+m=7, with Internal XOR-Gate LFSR Realization of the PRPG, (the Characteristic Polynomial, $f(x) = x^6 \oplus x^5 \oplus x^3 \oplus x^2 \oplus 1$).

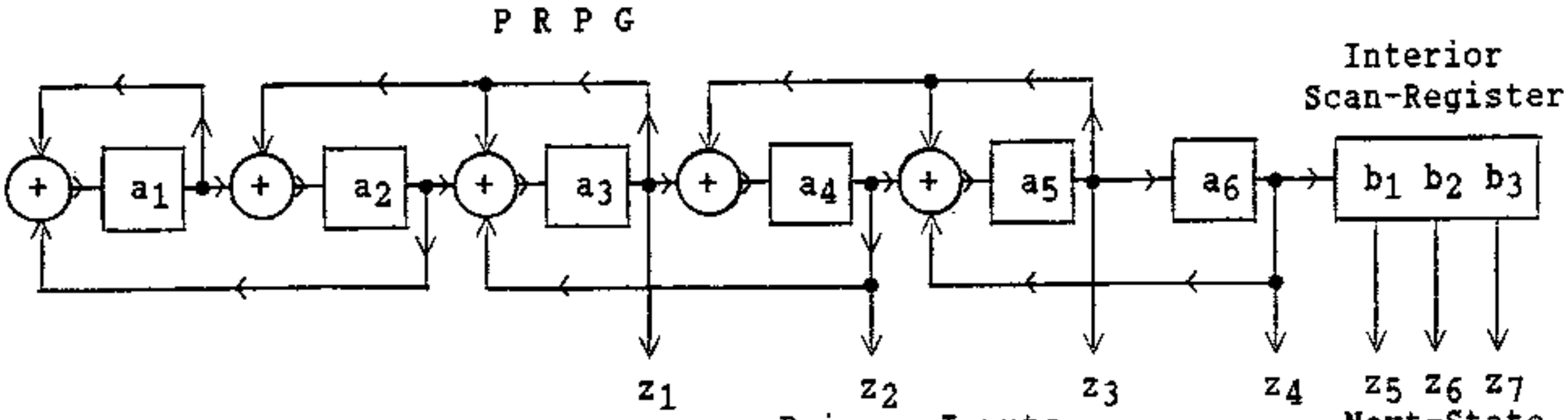

Fig. 4. An example of Efficient Test Generation: (s,n,m)=(6,4,3), r=n+m=7 with Cellular Automata Register (CAR) Realization of the PRPG, (the Characteristic Polynomial, $f(x) = x^6 \oplus x^5 \oplus x^3 \oplus x^2 \oplus 1$).

Consider a general block diagram of the proposed test generation for BIST boundary scan design (Fig. 5). The system consists of an autonomous linear

sequential circuit (ALSC) without feedforward, cascaded with a scan register, (e.g., see Fig 2, 3 and 4, where the ALSC is an LFSR and a cellular automata register, CAR[5,6]). We will show that for such a system there exists a one-to-one correspondence between $\underline{a}(t-k)$, the states of the ALSC at moments $t-k$ ($t \geq k$), and $\underline{y}(t)$, the contents of the first s consecutive bits of the r-bit test pattern at moments $t \geq k$, where $r \geq s$, $r=n+m$, and the initial state of the ALSC is denoted as $\underline{a}(0)$.

More specifically, the following theorem holds:

Theorem 1. For any ALSC without feedforwards, cascaded with a scan register,

$$\underline{y}(t+k) = C\underline{a}(t), \tag{1}$$

where $t \geq k$, $\underline{a}(t), \underline{y}(t) \in V_s$ (V_s denotes the s-dimensional vector space over $\{0,1\}$), and C is an $(s \times s)$ upper triangular matrix over GF(2) with det C = 1. (GF(2) is the Galois Field of two elements $\{0,1\}$ where the addition is the exclusive OR).

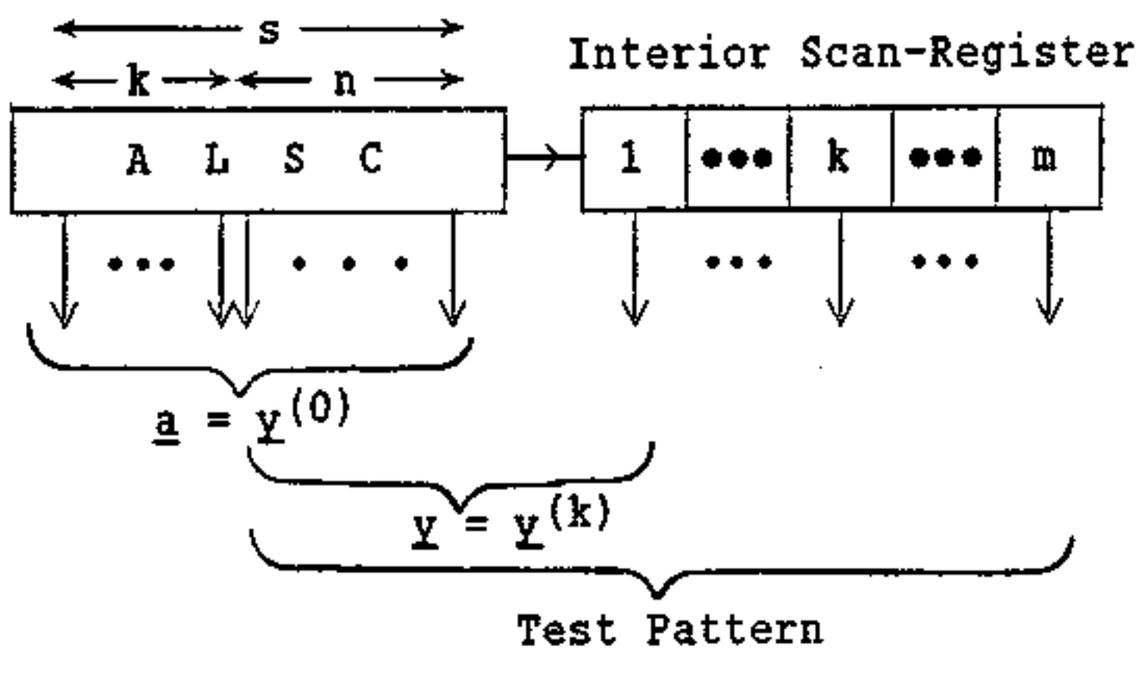

Fig. 5. Block Diagram of Test Generation for Boundary Scan

Proof. Denote by $\underline{y}^{(i)}(t)$; $i \in \{0,\ldots,k\}$, $k=s-n$, $\underline{y}^{(i)}(t) \in V_s$, the s-dimensional binary vector formed by the contents of the s-i last (rightmost) consecutive cells of the ALSC and i first (leftmost) cells of the scan register.

Let t be the initial moment of time. By definition, $\underline{y}^{(0)}(t) = \underline{a}(t)$. It is easy to see that for the moment of time t+i the vector $\underline{y}^{(i)}(t+i)$ is uniquely determined by the vector $\underline{y}^{(i-1)}(t+i-1)$. Namely,

$$\underline{y}^{(i)}(t+i) = C^{(i)}\underline{y}^{(i-1)}(t+i-1), \tag{2}$$

where $C^{(i)}$ is an upper triangular matrix with diagonal elements equal to one.

Indeed, denote by $y_j^{(i)}(t+i)$ the jth component (from left to right) of the vector $\underline{y}^{(i)}(t+i)$. Then, because of the absence of feedforwards, $y_j^{(i)}(t+i)$ is determined only by the components $y_g^{(i-1)}(t+i-1)$ with $g \geq j$. Moreover, $y_j^{(i-1)}(t+i-1)$ always contributes to $y_j^{(i)}(t+i)$ for the ALSC considered.

Hence, by recursive substitution, we obtain

$$\underline{y}(t+k) = \underline{y}^{(k)}(t+k) = C\underline{a}(t), \ (k=s-n), \tag{3}$$

where $C = C^{(k)}C^{(k-1)}\cdots C^{(1)}$, and C is also an upper triangular matrix with all the diagonal elements equal to one. Thus, C is a nonsingular matrix. Therefore, $\underline{a}(t)$ is uniquely determined by $\underline{y}(t+k)$

$$\underline{a}(t) = C^{-1}\underline{y}(t+k), \tag{4}$$

which implies that for different states $\underline{a}(t)$ of the ALSC the corresponding s-bit patterns $\underline{y}(t+k)$ are also different. □

Since all the 2^s-1 successive states of a PRPG with nonzero initial state (implemented as an ALSC) $\underline{a}(t)$, $t=0,\ldots,2^s-2$, are different, it follows from Theorem 1 that all the 2^s-1 successive r-bit patterns generated at the moments of time $t = k,k+1,\ldots,k+2^s-2$ are also different. Thus, after $k+2^s-1$ clocks the system will generate the maximum possible number of 2^s-1 different test patterns.

Example 1. Consider the case $(s,n,m) = (6,4,3)$, i.e., $r=7$ and $k=2$. Fig. 2, 3 and 4 show diagrams of three different realizations of PRPGs. For the case of the PRPG implemented by the external XOR-gates LFSR (see Fig. 2), it is obvious that the leftmost six-bit block of the test pattern $(z_1,\ldots,z_6)$ is the state of the PRPG delayed by k=2. This relation establishes the one-to-one correspondence.

For the PRPG being implemented by the internal XOR-gate LFSR (see Fig. 3), we have, $\underline{y}^{(0)}(t) = \underline{a}(t)$, and

$$\underline{y}^{(1)}(t+1) = \begin{pmatrix} y_1^{(1)}(t+1) \\ y_2^{(1)}(t+1) \\ y_3^{(1)}(t+1) \\ y_4^{(1)}(t+1) \\ y_5^{(1)}(t+1) \\ y_6^{(1)}(t+1) \end{pmatrix} = \begin{pmatrix} a_2(t+1) \\ a_3(t+1) \\ a_4(t+1) \\ a_5(t+1) \\ a_6(t+1) \\ b_1(t+1) \end{pmatrix} = \begin{pmatrix} 100000 \\ 010001 \\ 001001 \\ 000100 \\ 000011 \\ 000001 \end{pmatrix} \begin{pmatrix} y_1^{(0)}(t) \\ y_2^{(0)}(t) \\ y_3^{(0)}(t) \\ y_4^{(0)}(t) \\ y_5^{(0)}(t) \\ y_6^{(0)}(t) \end{pmatrix} = \begin{pmatrix} 100000 \\ 010001 \\ 001001 \\ 000100 \\ 000011 \\ 000001 \end{pmatrix} \begin{pmatrix} a_1(t) \\ a_2(t) \\ a_3(t) \\ a_4(t) \\ a_5(t) \\ a_6(t) \end{pmatrix}$$

$$= C^{(1)}\underline{y}^{(0)}(t) = C^{(1)}\underline{a}(t). \tag{5}$$

$$\underline{y}^{(2)}(t+2) = \begin{pmatrix} y_1^{(2)}(t+2) \\ y_2^{(2)}(t+2) \\ y_3^{(2)}(t+2) \\ y_4^{(2)}(t+2) \\ y_5^{(2)}(t+2) \\ y_6^{(2)}(t+2) \end{pmatrix} = \begin{pmatrix} a_3(t+2) \\ a_4(t+2) \\ a_5(t+2) \\ a_6(t+2) \\ b_1(t+2) \\ b_2(t+2) \end{pmatrix} = \begin{pmatrix} 100010 \\ 010010 \\ 001000 \\ 000110 \\ 000010 \\ 000001 \end{pmatrix} \begin{pmatrix} y_1^{(1)}(t+1) \\ y_2^{(1)}(t+1) \\ y_3^{(1)}(t+1) \\ y_4^{(1)}(t+1) \\ y_5^{(1)}(t+1) \\ y_6^{(1)}(t+1) \end{pmatrix}$$

$$= C^{(2)}\underline{y}^{(1)}(t+1) = C^{(2)}C^{(1)}\underline{a}(t). \tag{6}$$

For the PRPG implemented by the cellular automata register (CAR), (see Fig. 4), we have,

$$C^{(1)} = \begin{pmatrix} 101000 \\ 011100 \\ 001010 \\ 000111 \\ 000010 \\ 000001 \end{pmatrix}, \quad C^{(2)} = \begin{pmatrix} 111000 \\ 010100 \\ 001110 \\ 000100 \\ 000010 \\ 000001 \end{pmatrix}, \quad C^{(3)} = \begin{pmatrix} 101000 \\ 011100 \\ 001000 \\ 000100 \\ 000010 \\ 000001 \end{pmatrix},$$

$$C^{(4)} = \begin{pmatrix} 111000 \\ 010000 \\ 001000 \\ 000100 \\ 000010 \\ 000001 \end{pmatrix}, \quad C^{(5)} = \begin{pmatrix} 100000 \\ 010000 \\ 001000 \\ 000100 \\ 000010 \\ 000001 \end{pmatrix}, \quad C^{(6)} = \begin{pmatrix} 100000 \\ 010000 \\ 001000 \\ 000100 \\ 000010 \\ 000001 \end{pmatrix}. \tag{7}$$

All $C^{(i)}$, (i=1,...,6, in this example $k \leq 6$, s=6), are nonsingular over GF(2).

In contrast, if the connection points to the PIs are taken from the first four cells of the CAR the state-dependence equation for the first s-bit block of the r-bit test patterns (s=6, r=7) is given by

$$\begin{pmatrix} z_1 \\ z_2 \\ z_3 \\ z_4 \\ z_5 \\ z_6 \end{pmatrix} = \begin{pmatrix} 100000 \\ 010000 \\ 001000 \\ 000100 \\ 111011 \\ 011111 \end{pmatrix} \begin{pmatrix} a_1 \\ a_2 \\ a_3 \\ a_4 \\ a_5 \\ a_6 \end{pmatrix}. \tag{8}$$

The above matrix over GF(2) is singular which implies that the 2^s-1 successive r-bit test patterns are not guaranteed to be all distinct. In fact, only 33% of the r-bit patterns generated by application of $s-n+2^s-1$ clock pulses were distinct.[5,6] □

DECIMATION OF TEST PATTERNS BY NEXT STATE RESPONSES

The second problem lies in the decimation of the test patterns due to the fact that the contents of the interior register are replaced by the next state responses after the test patterns are applied to the chip-under-test. To minimize the test time we proposed that a new m-bit pattern for the interior register is being shifted in while the the next state response is being shifted out. As a consequence, the r-bit test patterns applied to the chip-under-test correspond to the states of the PRPG appearing at the intervals of m clock pulses. It was shown that the period of the state transition of an autonomous linear sequential circuit (ALSC) when sampled at an interval of m clock pulses is equal to the period of ALSC divided by the greatest common divisor of m and the period of the ALSC[8]. Hence, the number of r-bit test patterns attainable is equal to 2^s-1 if m and 2^s-1 are relatively prime, that is, $\gcd(m,2^s-1) = 1$.

In the event that the length m of the interior register is not relatively prime to 2^s-1 we can introduce at every test cycle a number δ of "dummy" shifts to the PRPG and the interior register, the signature analyzer input being at that time disabled, such that $m+\delta$ is relatively prime to 2^s-1 and therefore be able to achieve a full pattern coverage. Moreover, the number δ is typically very small such as one or two. These additional shifts give rise to an overhead in the test time. However, when compared to an approach using an additional register and a multiplexer our approach is more versatile, since it does not require any changes in the chip design.

Example 2. In Example 1, the parameters of the BIST scheme were (s,n,m) = (6,4,3). Hence, at every test cycle, while the next state response is being scanned into the signature analyzer, a new interior-register test pattern generated by the PRPG is at the same time being scanned-in. Thus, a new test pattern appears after m = 3 state transitions. In this case, only $(2^s-1)/\gcd(m,2^s-1) = 63/\gcd(3,63) = 21$ of the 7-bit test patterns (r = n+m = 7) can be generated. However, with one addition clock pulse at every test cycle (δ = 1), the PRPG now undergoes 4 state transitions for every test cycle and the number of 7-bit test patterns that can be generated is 63, since $m+\delta = 4$ is relative prime to $2^s-1 = 63$. In this example, we can obtain a full patterns coverage at the expense of 63 extra clock pulses without additional hardware. □

Efficient Test Generation for the Case When r<s

In the design of a specific chip, a designer may have to use a pre-design boundary-scan template in which the number of PRPG flip-flops s is greater than the number of bits r in the test patterns. The problem arises as how to efficiently generate, with a minimal number of clock pluses, a desired number $T \le 2^r$ distinct r-bit patterns using s-stage PRPG when r<s. (An inefficient technique is to clock the PRPG for 2^s-1 times). The efficiency of a test generation (when s, r and T are given) depends on the choice of the initial state of the PRPG. For ramdomly chosen initial state, we can characterize the efficiency in terms of $\bar{N}(T)$, the expected number of clock pulses (over an ensemble of s-stage PRPGs and their initial states) such that a PRPG will generate $T \le 2^r$ r-bit patterns, and $\bar{T}(N)$, the expected number of distinct r-bit patterns generated within N clock pulses. We note also that the problem of determining an initial state that results in a minimal number of clock pulses for a given s-stage PRPG generating $T \le 2^r$ r-bit

patterns is still open.

The proposed probabilistic model for the test generation procedure is a repeated experiment of randomly drawing, without replacement, an r-bit pattern out from the pool initially containing 2^s r-bit patterns distributed uniformly. The assumption made is that an r-bit pattern generated by PRPG at any moment of clock pulse is random (random draws). Moreover, since the r-bit patterns are the r consecutive bits of the s-bit patterns generated by the PRPG, it follows that, with 2^s-1 clock pluses every nonzero r-bit pattern appears 2^{s-r} times and the pattern of r zero's appears $2^{s-r}-1$ times, thus, the proposed model is assumed as a drawing without-replacement experiment. (The random without replacement drawing model has been used in [10] for estimating the number of pseudorandom patterns needed to achieve a given fault coverage for pseudorandom testing).

In the proposed model, let v be a random variable defined as the number of draws (analogous to the number of clock pulses) and τ be a random variable defined as the number of distinct patterns appeared. We estimate in Theorem 2, below, the expected number $\bar{N}(T)$ of random draws such that T distinct patterns will appear for the first time. Moreover, the expected number $\bar{T}(N)$ of distinct patterns appeared in N draws ($v=N$) is given below in Corollary 1. (Proofs of Theorem 2 and Corollary 1 are given in the appendix).

Theorem 2. Let $Q = 2^r$, $M = 2^{s-r}$ and ξ_i be a binary random variable defined as follows; $\xi_i=1$ if the pattern appeared at the ith draw has not previously appeared (distinct) and $\xi_i=0$ if the pattern has previously appeared. The conditional probability that exactly T distinct patterns will appear within N random draws satisfies the folowing equation:

$$\Pr\{\tau=T \mid v=N\} = \Pr\{\tau=T \mid v=N-1\}\Pr\{\xi_N=0\} + \Pr\{\tau=T-1 \mid v=N-1\}\Pr\{\xi_N=1\}, \quad (9)$$

where $\Pr\{\xi_N=0\} = \frac{MT-N+1}{MQ-N+1}$ and $\Pr\{\xi_N=1\} = \frac{M(Q-T+1)}{MQ-N+1}$.

The solution of the above functional equation is:

$$\Pr\{\tau=T \mid \upsilon=N\} = \binom{MQ}{N}^{-1} \binom{Q}{T} \sum_{\ell=0}^{T} (-1)^{T-\ell} \binom{T}{\ell} \binom{M\ell}{N} . \tag{10}$$

The conditional probability that N is a number of draws such that $1 \le T \le Q$ distinct patterns will appear for the first time (minimal number of draws) is given by

$$\Pr\{\upsilon=N \mid \tau=T\} = \Pr\{\tau=T-1 \mid \upsilon=N-1\}\Pr\{\xi_N=1\}, \tag{11}$$

and the conditional expected value for the number of draws given T, $(1 \le T \le Q)$, is

$$E\{\upsilon \mid \tau=T\} = \bar{N}(T) = (MQ+1)\left[1 - \prod_{k=Q-T+1}^{Q} (1 + \frac{1}{Mk})^{-1}\right]. \tag{12}$$

A good approximation for $\bar{N}(T)$ when $Q \gg 1$ can be given by:

$$\bar{N}(T) \approx \begin{cases} (MQ+1)\left[1 - (Q(Q-T)^{-1})^{-1/M} \exp([2M(Q-T)]^{-1} - (2MQ)^{-1})\right], & T<Q; \\ (MQ+1)\left[1 - Q^{-1/M} \exp(-\gamma M^{-1})\right], & T=Q; \end{cases} \tag{13}$$

where $C \approx 0.577$ is the Euler's constant[11]. □

Corollary 1. The conditional expected value for the number of distinct patterns given $\upsilon = N$,

$$E\{\tau \mid \upsilon=N\} = \bar{T}(N) = Q - Q\binom{MQ}{N}^{-1}\binom{MQ-M}{N}. \tag{14}$$

□

Fig. 6 and 7, (below), show a comparison of $\bar{N}(T)$ and the simulation results $\bar{N}_{ex}(T)$ for s = 16, r = 8, 10, and 14; and, s = 24, r = 14, 18 and 22, where the characteristic polynomials of the PRPGs are $x^{16} \oplus x^5 \oplus x^3 \oplus x^2 \oplus 1$ and $x^{24} \oplus x^7 \oplus x^2 \oplus x \oplus 1$ repectively. The average values $\bar{N}_{ex}(T)$ have been obtained from 20 randomly chosen initial states of the PRPG and three different realizations of the PRPG: the external XOR-gate LFSR, the internal XOR-gate LFSR, and the cellular automata register (CAR). The comparison of $\bar{N}(T)$ and $\bar{N}_{ex}(T)$

are shown in terms of the efficiency for the test generation $\bar{N}(T)/T$ and $\bar{N}_{ex}(T)/T$ versus the normalized value $T/2^r$, futhermore, the functions $\bar{N}(T)$ are shown in the solid lines and $\bar{N}_{ex}(T)$ are shown as data points, with different symbols for different r values, indicating the experimental averages and the standard deviations.

The experimental results, $\bar{N}_{ex}(T)$ obtained for s = 16, s = 24, and wide range of r values indicate that, the proposed $\bar{N}(T)$ provides a good theoretical estimate for an average number of clock pulses over randomly chosen the initial states of the PRPG. We also observe that the exhaustive test generation of all 2^r r-bit patterns (i.e., $T/2^r = 1$) can be quite inefficient where as the cases of "near" exhautive test generation (e.g., $T/2^r = 0.95$) are reasonablely efficient.

We presented a modified internal connections of BIST boundary-scan template which ensures a full patterns coverage for the case when $r \geq s$. The modification from the original circuitry is that, the connections for PIs are from the last n consecutive cells of the PRPG. It is important to note that, the proposed modification is independent on the choice of PRPG implementation.

For the case when $r < s$, the expected number $\bar{N}(T)$ of PRPG clock pulses required for generating $T \leq 2^r$ distinct r-bit patterns and the expected number $\bar{T}(N)$ of distinct patterns given a number N of clock pulses were presented. The proposed theoretical average $\bar{N}(T)$ is proven to be close to the experimental average values $\bar{N}_{ex}(T)$ for s = 16 and 24, and wide range of r values. Hence, the value $\bar{N}(T)$ or $\bar{T}(N)$ can be used as a benchmark for evaluating the choice of PRPG parameters and initial states.

$\frac{\overline{N}(T)}{T}$; $\frac{\overline{N}_{ex}(T)}{T}$, o: r=8, ◇: r=10, Δ: r=14

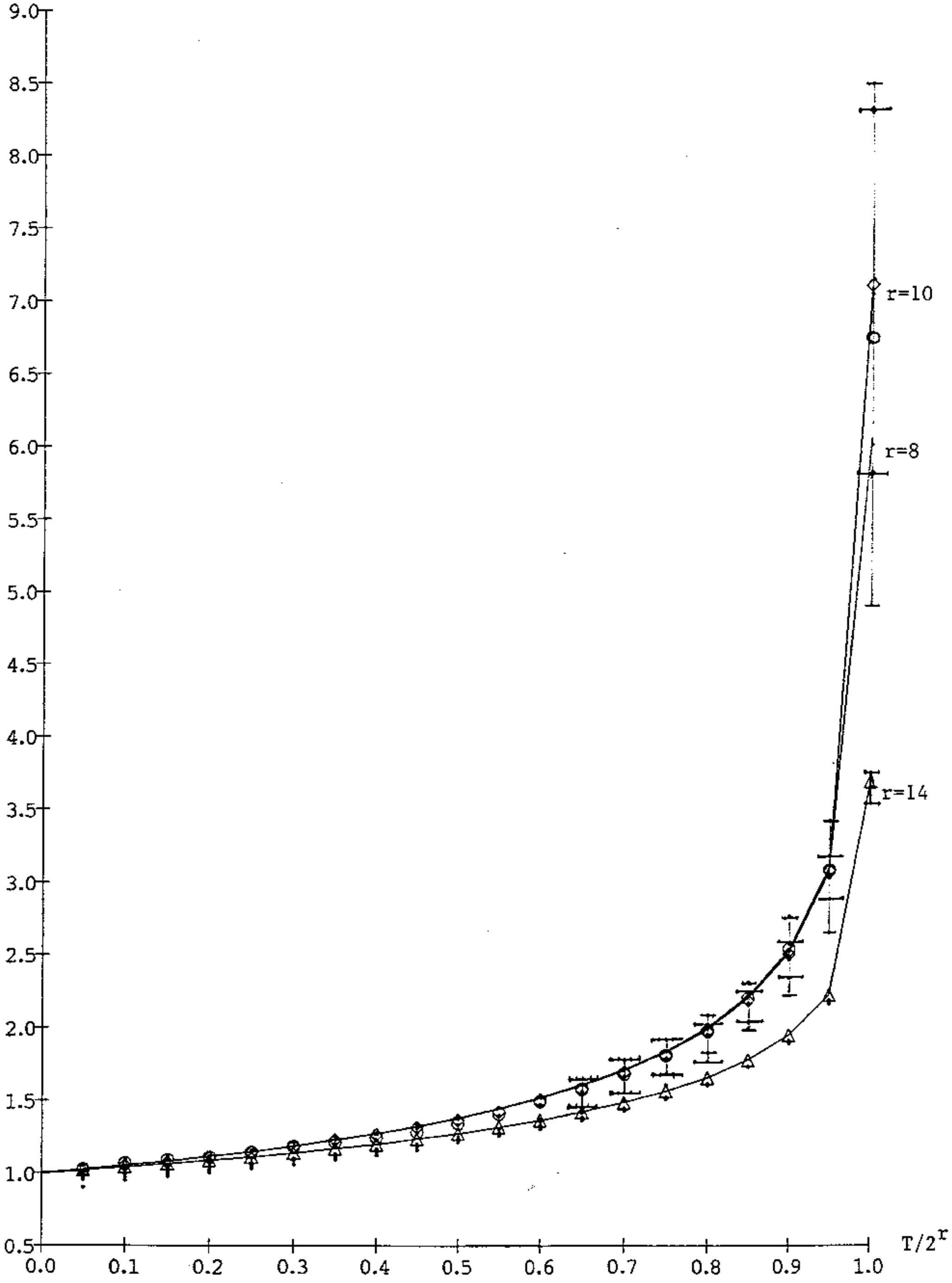

Fig. 6. $\frac{\overline{N}(T)}{T}$ (lines) and $\frac{\overline{N}_{ex}(T)}{T}$ (data points) for s=16; r = 8, 10 and 14

$\frac{\overline{N}(T)}{T}$; $\frac{\overline{N}_{ex}(T)}{T}$, o: r=14, ◇: r=18, Δ: r=22

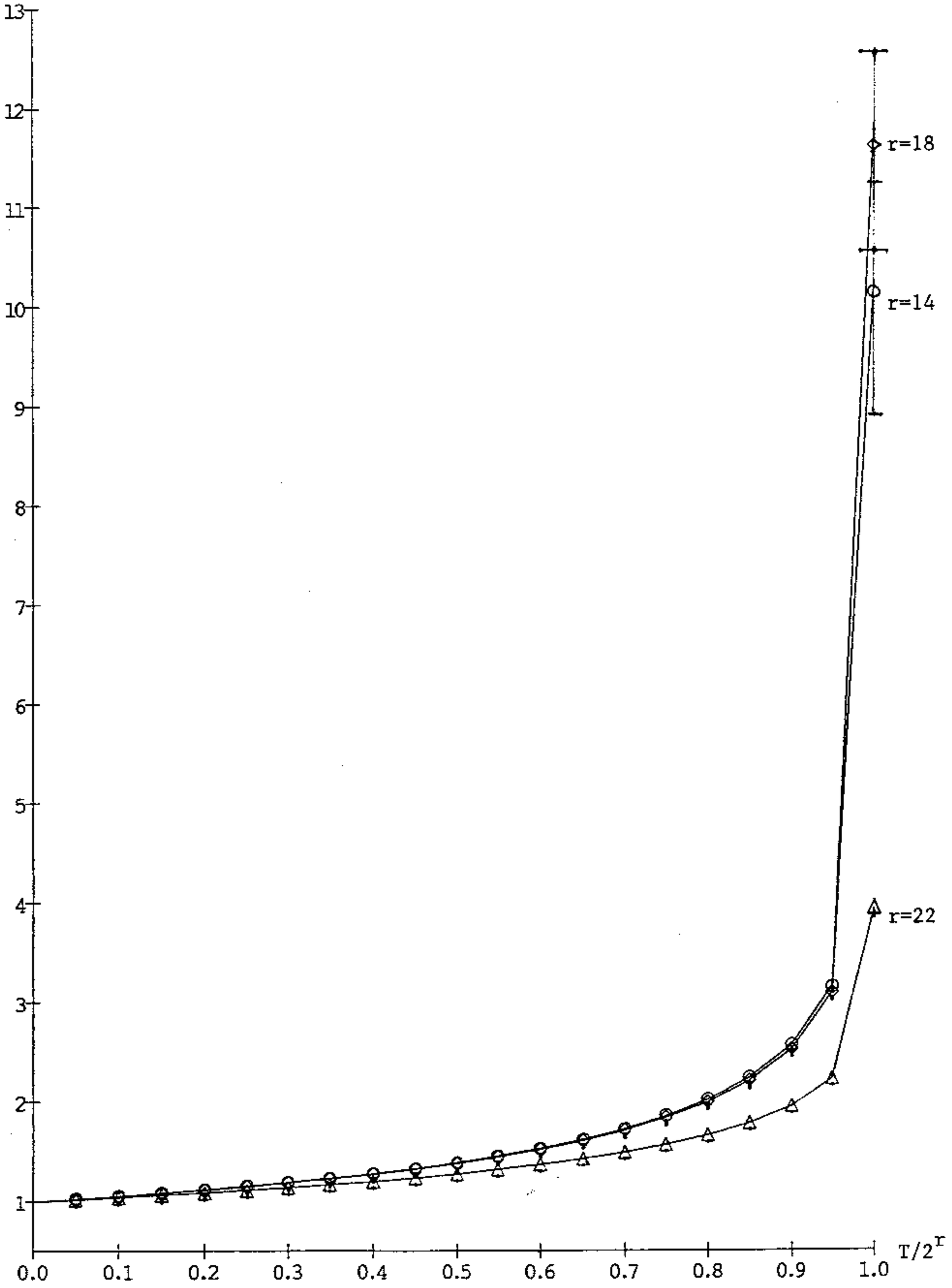

Fig.7. $\frac{\overline{N}(T)}{T}$ (lines) and $\frac{\overline{N}_{ex}(T)}{T}$ (data points) for s=24, r = 14, 18 and 22

Appendix

Proof of Theorem 2. In (9), $\Pr\{\tau=T|\nu=N\}$ is expressed as a sum of two probabilities: $\Pr\{\tau=T|\nu=N-1\}\Pr\{\xi_N=0\}$, the probability that T distinct patterns appear before the Nth draw; and $\Pr\{\tau=T-1|\nu=N-1\}\Pr\{\xi_N=1\} = \Pr\{\nu=N|\tau=T\}$, the probability that in N draws T distinct pattern appear for the first time, (see, (11)). It can be verified that $\Pr\{\tau=T|\nu=N\}$ given in (10) satisfies (9) and the initial condition $\Pr\{\tau=1,\nu=0\} = 0$, $\Pr\{\tau=1,\nu=1\} = 1$.

The expected value $\bar{N}(T)$ given in (12) is obtained from

$$\bar{N}(T) = \sum_{N=0}^{MQ} N \Pr\{\tau=T-1|\nu=N-1\} \frac{M(Q-T+1)}{MQ-N+1}$$

$$= (MQ+1)\left[1 - \frac{Q!\Gamma(Q-T+1+1/M)}{(Q-T)!\Gamma(Q+1+1/M)}\right], \qquad (15)$$

where $\Gamma(x)$ is the Euler Gamma-function.[11]

For $Q>>1$ we have, the term, (see, (12)),

$$\prod_{k=Q-T+1}^{Q}(1+\frac{1}{Mk})^{-1} \geq \exp(-\frac{1}{M}\sum_{k=Q-T+1}^{Q}k^{-1}) = \exp(-\frac{1}{M}[\psi(Q+1)-\psi(Q-T+1)]), \qquad (16)$$

where $\psi(x) = d\ln\Gamma(x)/dx$.[12] Finally, the approximations (13) are obtained from (16) using a series expansion for $\psi(x)$.[11] □

Proof of Corollary 1. Let $\{\nu_i, i=1,\ldots,Q\}$ be a set of random variables defined as the number of times the patterns from the pool of Q patterns will appear in N draws, $(\nu_1+\nu_2+\ldots+\nu_Q = N,\ \nu_i\geq 0)$, then, we have,

$$\Pr\{\nu_i\geq 1\} = 1 - \binom{MQ}{N}^{-1}\binom{MQ-M}{N}. \qquad (17)$$

Further, let us define a set of binary random variables, $\{\zeta_i: \zeta_i=1 \text{ iff } \nu_i\geq 1, i=1,\ldots,Q\}$, then, the expected value, $E\{\zeta_i\} = \Pr\{\nu_i\geq 1\}$. Finally, (14) is obtained by

$$\bar{T}(N) = E\{\sum_{i=1}^{Q} \zeta_i\} = \sum_{i=1}^{Q} E\{\zeta_i\} = Q \Pr\{v_i \geq 1\} = Q - Q\binom{MQ}{N}^{-1}\binom{MQ-M}{N}. \quad (18)$$

Note that, $\bar{T}(N)$ can also be found by taking the expectation of T,

$$\bar{T}(N) = \sum_{T=0}^{\min\{N,Q\}} T \Pr\{\tau=T \mid v=N\}, \quad (19)$$

where $\Pr\{\tau=T \mid v=N\}$ is given by (10). □

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