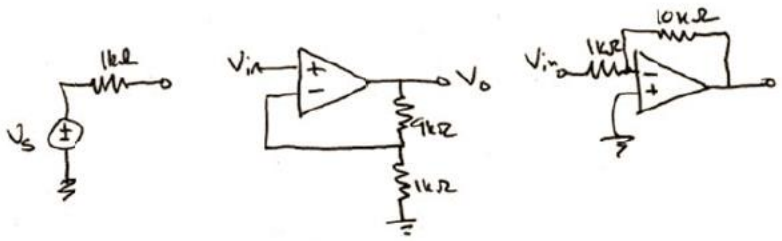
EK307 Fall 2017 Homework 5 Solutions

Problem 1:



Circuit 1 Circuit 2

a) Non-inverting config. Inverting config

Gain: $A = 1 + \frac{9k\Omega}{1k\Omega} = 10$ Gain $A = -\frac{10k\Omega}{1k\Omega} = -10$

both amplifiers have a gain of 10 or -10 without the source connected.

b) When the source is connected the non-inverting amplifier is unchanged. The inverting amplifier absorbs the 1kΩ of the source into its input resistance.

The gain of the inverting amplifier is now:

$$A = -\frac{10k\Omega}{1k\Omega + 1k\Omega} = -5$$

Problem 2:

Design a circuit with one op-amp that provides a gain of 5.5. Assume you have a resistor Ri =10kΩ, what value would you choose for Rf?

The gain here is positive hence it is a non inverting amplifier.

$$V_{in} = \frac{R_i}{R_i + R_f} \times V_{out}$$

Ideal summing point: $V_1 = V_{in}$

Voltage gain A is equal to: $\frac{V_{out}}{V_{in}}$

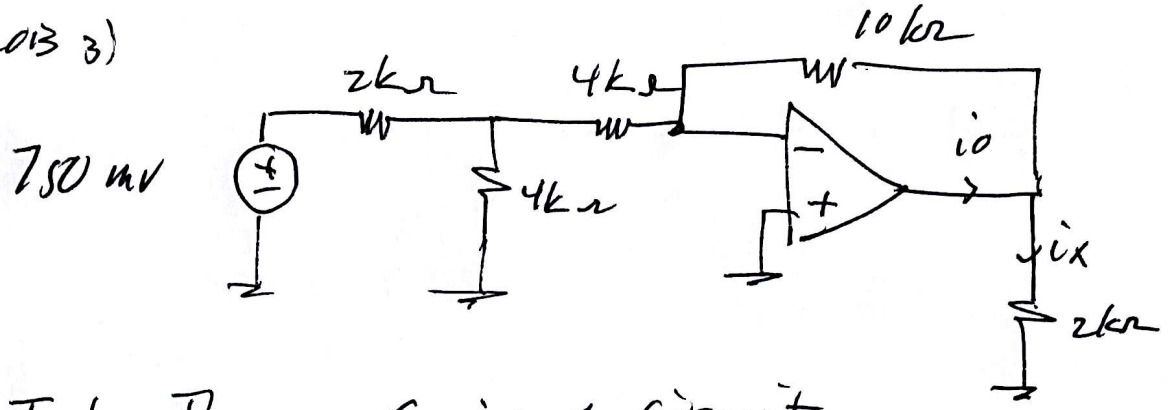
Then, $A = \frac{V_{out}}{V_{in}} = \frac{R_i + R_f}{R_i}$

Transpose to give , $A = \frac{V_{out}}{V_{in}} = 1 + \frac{R_f}{R_i}$

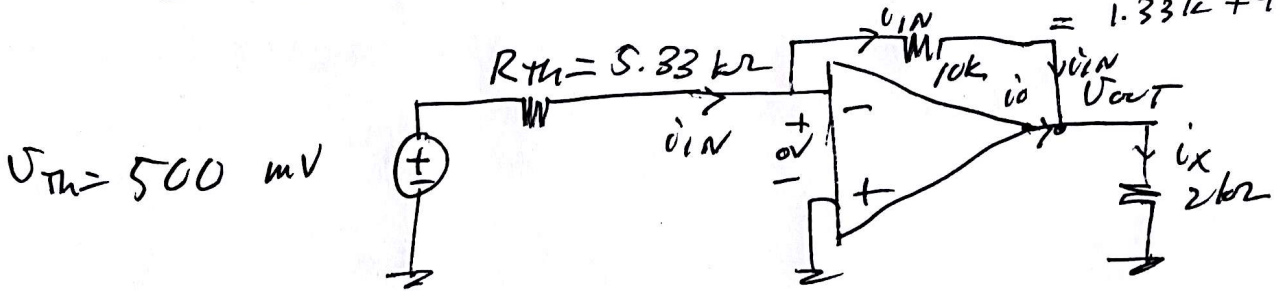
$$5.5 = 1 + \frac{R_f}{10}$$

Therefore $R_f = 45\ K\Omega$

PROB 3)



Take Thevenin Equiv of circuit connected to V− terminal: (R_{Th} = 2k||4k + 4k = 1.33k + 4k = 5.33kΩ



$$i_{IN} = \frac{500\,mV}{5.33\,k\Omega} = 93.7\,\mu A$$

$$V_{OUT} = \frac{10k\Omega}{5.33k\Omega} \times 500\,mV = -937\,mV \checkmark$$

$$i_x = \frac{V_{OUT}}{2k\Omega} = \frac{-937\,mV}{2\,k\Omega} = -468\,\mu A$$

KCL at V_{OUT} NODE:

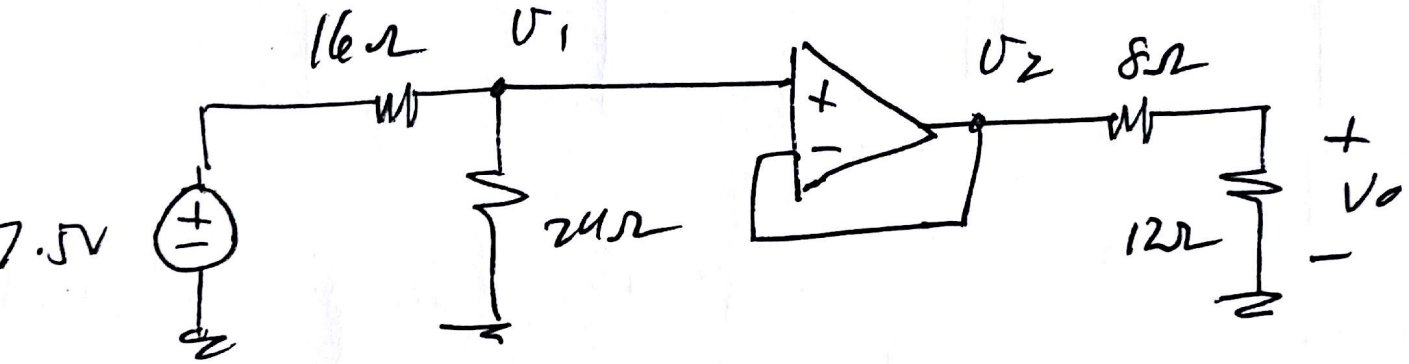
$$i_{IN} + i_o - i_x = 0$$

$$i_o = i_x - i_{IN}$$

$$= -468\,\mu A - 93.7\,\mu A = -562\,\mu A = i_o$$

(ROBY)

Voltage follower $v_2 = v_1$

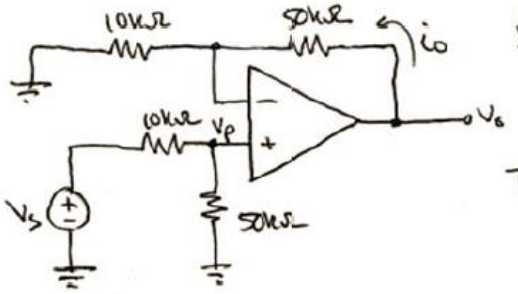


VOLTAGE DIVISION:

$$v_1 = \frac{24}{16+24} \times 7.5 = 4.5V = v_2$$

$$v_o = \frac{12}{12+8} v_2 = \frac{12}{12+8} 4.5 = 2.7V$$

Problem 5:



Find V_o in terms of V_s
i_o when $V_s = 2V$

This is a difference Amplifier
with $V_1 = 0$, $V_2 = V_s$

OR

A non-inverting amplifier with
a voltage divider on the input.

As a non-inverting Amp,

$$V_o = V_p\left(1 + \frac{50k\Omega}{10k\Omega}\right) = 6V_p.$$

$$V_p = V_s\left(\frac{50k\Omega}{10k\Omega + 50k\Omega}\right) = \frac{5}{6}V_s$$

$$V_o = 6V_p = 6\left(\frac{5}{6}V_s\right) = 5V_s$$

As a difference Amplifier

$$V_o = V_1\left(-\frac{R_2}{R_1}\right) + V_2\left(\frac{R_1+R_2}{R_1}\right)\left(\frac{R_4}{R_3+R_4}\right)$$

$$= 0 + V_2\left(\frac{10k\Omega+50k\Omega}{10k\Omega}\right)\left(\frac{50k\Omega}{50k\Omega+10k\Omega}\right)$$

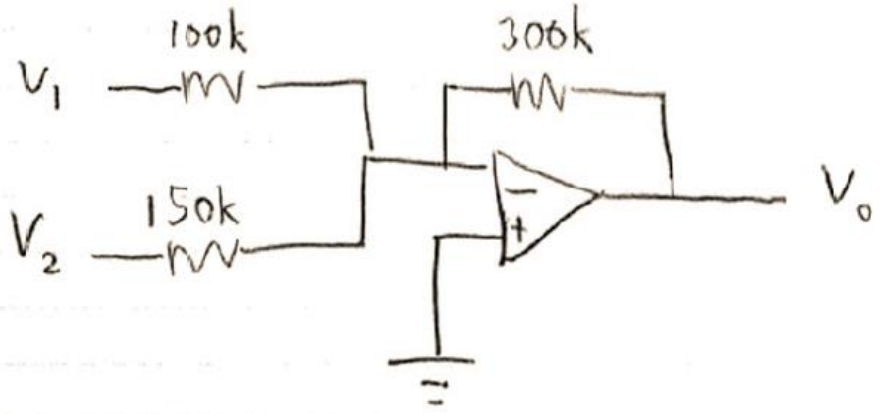
$$= 5\cdot V_2 = 5\cdot V_s$$

$$i_o = \frac{V_o}{50k\Omega+10k\Omega} = \frac{5\cdot V_s}{60k\Omega}$$

$$\boxed{V_s = 2 \rightarrow \quad i_o = 167\mu A}$$

Problem 6:

This is an inverting summer, which could be redrawn



So

$$V_o = -\frac{300}{100}V_1 - \frac{300}{150}V_2$$

$$= -3V_1 - 2V_2$$

$V_1 = 1 \Rightarrow V_o = -3 - 2V_2$

for linear operation, we require

$$-15 < V_o < 15$$

$$-15 < -3 - 2V_2 < 15$$

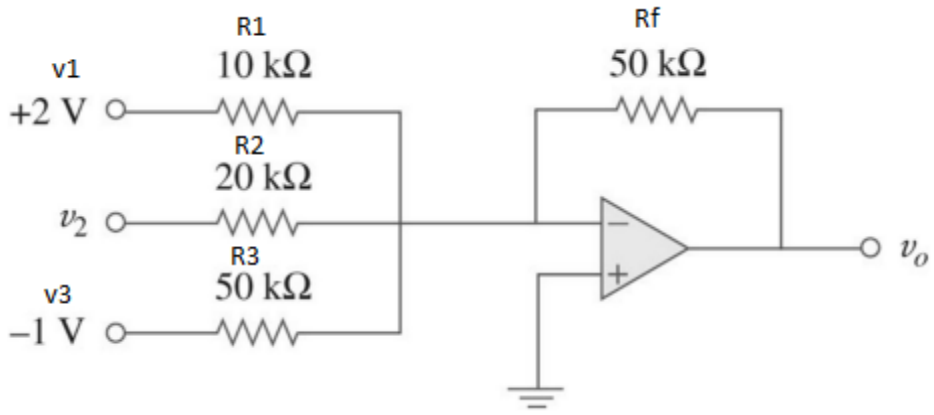
$$-12 < -2V_2 < 18$$

$$\boxed{6 > V_2 > -9}$$

Problem 7:

The circuit shown is a summing amplifier.

The resistances are labelled as,



The formula to calculate the value of v_0 in this summing amplifier circuit is,

$$v_0 = -\left[\frac{R_f}{R_1} \times v_1 + \frac{R_f}{R_2} \times v_2 + \frac{R_f}{R_3} \times v_3\right]$$

Substituting the known values,

$$v_0 = -\left[\frac{50}{10} \times 2 + \frac{50}{20} \times v_2 + \frac{50}{50} \times (-1)\right]$$

$$= -[10 + 2.5v_2 - 1]$$

$$v_0 = -9 - 2.5v_2$$

Substituting the desired value $v_0 = -16.5\ v$

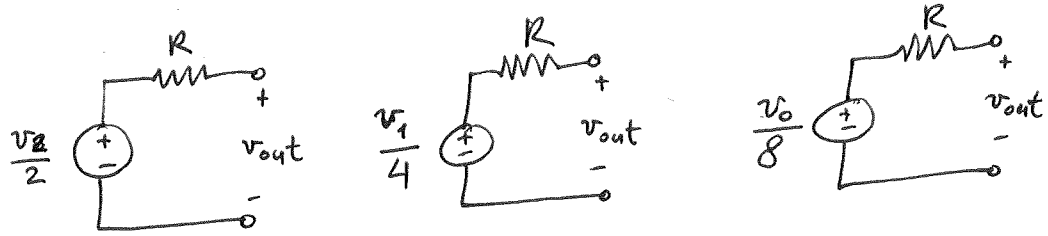
$$-16.5 = -9 - 2.5v_2 \quad \rightarrow \quad v_2 = 3V$$

PROBLEM 8 : R-2R DAC, PART II

(a) FROM HOMEWORK #4, PROBLEM 10, THE THÉVENIN EQUIVALENTS FOR EXCITATIONS OF EACH SOURCE SEPARATELY ARE:

INPUT: $(v_2, 0, 0)$ $(0, v_1, 0)$ $(0, 0, v_0)$

THEVENIN EQUIV:



BY SUPERPOSITION, THE VOLTAGE ON AN UNLOADED CIRCUIT FOR ANY INPUT (v_2, v_1, v_0) IS:

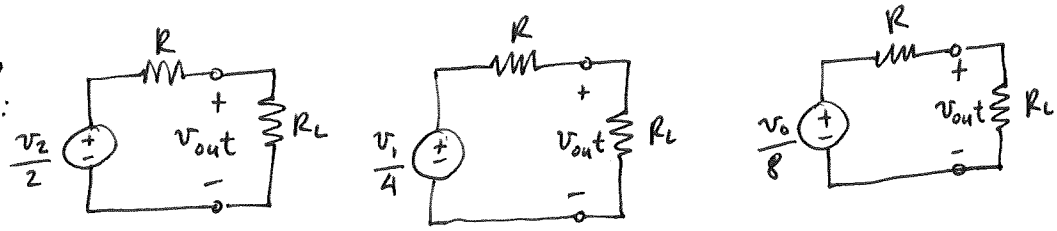
$$v_{out} = \frac{v_2}{2} + \frac{v_1}{4} + \frac{v_0}{8} = v_2 \cdot 2^{-1} + v_1 \cdot 2^{-2} + v_0 \cdot 2^{-3}$$

THIS SHOWS THAT IT PERFORMS THE FUNCTION OF A D/A CONVERTER WITH 3 BITS, WITH v_2 THE MOST SIGNIFICANT BIT (MSB), AND v_0 THE LEAST SIGNIFICANT BIT (LSB).

(b) WITH A LOAD R_L:

INPUT: $(v_2, 0, 0)$ $(0, v_1, 0)$ $(0, 0, v_0)$

THEVENIN EQUIV:



v_{out}: $v_{out} = \frac{R_L}{R+R_L}\frac{v_2}{2}$ $v_{out} = \frac{R_L}{R+R_L}\frac{v_1}{4}$ $v_{out} = \frac{R_L}{R+R_L}\frac{v_0}{8}$

THEREFORE:

$$v_{out} = \frac{R_L}{R+R_L}\frac{v_2}{2} + \frac{R_L}{R+R_L}\frac{v_1}{4} + \frac{R_L}{R+R_L}\frac{v_0}{8}$$

$$v_{out} = \frac{R_L}{R+R_L}\left(\frac{1}{2}v_2 + \frac{1}{4}v_1 + \frac{1}{8}v_0\right)$$

$$v_{out} = \frac{R_L}{R+R_L}\left(2^{-1}\cdot v_2 + 2^{-2}\cdot v_1 + 2^{-3}\cdot v_0\right)$$

FOR $R_L \to \infty$, WE GET THE RESULT IN PART (a).

Problem Set 5 Solutions

Problem 8.

(c) Figure C below is created by the attached Matlab script (file named s_hw5cdsoln.m). **The output voltage is lower for lower load resistor R_L.**

The DAC still works, and provides an output voltage that is linearly proportional to the digital input from 0 (000) to 7 (111). However, the proportionality factor depends on the load. The highest proportionality factor is for open circuit, and is lower for lower values of R_L. Thus, with variable R_L, the DAC does not put out the same voltage range.

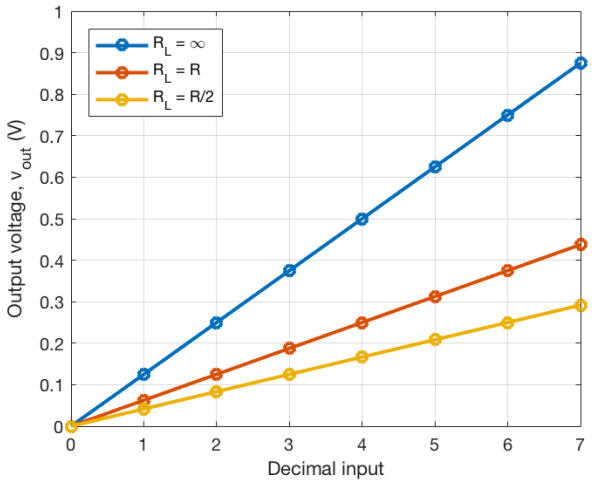


Figure C

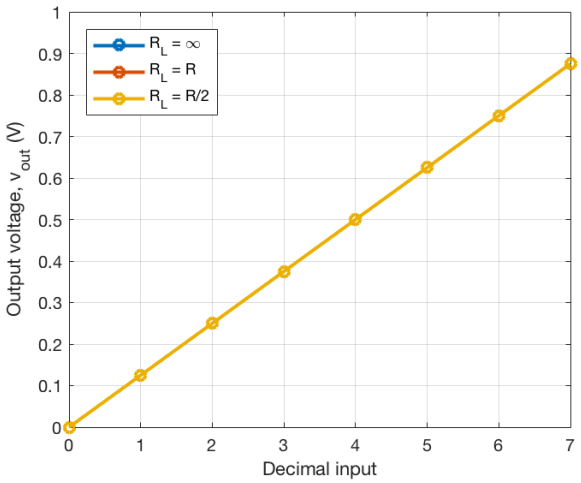
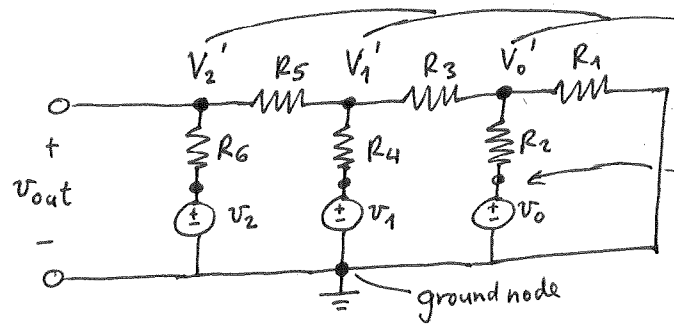


Figure D

(d) The addition of the unity-gain buffer means that the current into the op-amp is zero, so the DAC resistor network "sees" the op-amp as an infinite resistance, or open circuit. The voltage at the op-amp non-inverting input, though, is replicated by the op-amp output, which can provide that voltage no matter what load R_L is connected. So, we get the output voltage of the open circuit solution vout in part (a) for any value of connected R_L.

The plot in **Figure D**, above, from the solution Matlab script (file named s_hw5cdsoln.m), shows the 3 curves overlapping. **The unity-gain buffer helps make the output voltage range independent of the attached load resistance. And, the DAC still works like a DAC.**

(e)



INPUT: (v_2, v_1, v_0)

OUTPUT: v_{out}

THE CIRCUIT HAS 7 NODES: ONE IS GROUND, AND 3 ARE KNOWN (v_2, v_1, v_0). WE LABEL THE 3 UNKNOWN NODES V_2', V_1' AND V_0'. THE DESIRED OUTPUT VOLTAGE $v_{out} = V_2'$. THE NODE VOLTAGE EQUATIONS ARE:

$$\left(\frac{1}{R_1}+\frac{1}{R_2}+\frac{1}{R_3}\right)V_0' - \frac{1}{R_3}V_1' - \frac{1}{R_2}v_0 = 0$$

$$\left(\frac{1}{R_3}+\frac{1}{R_4}+\frac{1}{R_5}\right)V_1' - \frac{1}{R_3}V_0' - \frac{1}{R_5}V_2' - \frac{1}{R_4}v_1 = 0$$

$$\left(\frac{1}{R_5}+\frac{1}{R_6}\right)V_2' - \frac{1}{R_5}V_1' - \frac{1}{R_6}v_2 = 0$$

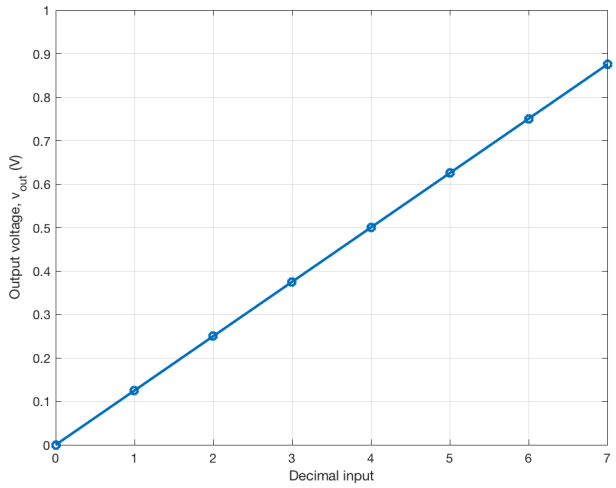
THE MATRIX EQUATION IS:

$$\begin{bmatrix} \frac{1}{R_1}+\frac{1}{R_2}+\frac{1}{R_3} & -\frac{1}{R_3} & 0 \\ -\frac{1}{R_3} & \frac{1}{R_3}+\frac{1}{R_4}+\frac{1}{R_5} & -\frac{1}{R_5} \\ 0 & -\frac{1}{R_5} & \frac{1}{R_5}+\frac{1}{R_6} \end{bmatrix} \begin{bmatrix} V_0' \\ V_1' \\ V_2' \end{bmatrix} = \begin{bmatrix} \frac{1}{R_2}v_0 \\ \frac{1}{R_4}v_1 \\ \frac{1}{R_6}v_2 \end{bmatrix}$$

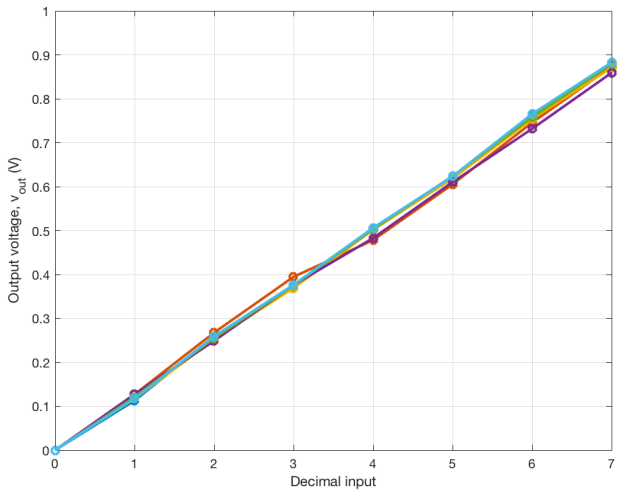
KNOWN — OUTPUTS — INPUTS/KNOWN

$v_{out} = V_2'$

(f) The code is attached (file named s_hw5_r2rdac_v3.m). It gives the function that solves the circuit using the matrix node-voltage method. The plot is:



(g) I chose to use 6 different cases, and plotted them below. The code is attached (file named s_hw5_r2rdac_v3_g.m). The code shows my choice of 6 resistors each time.



```
% Problem 8
clear all; close all;

% 8(c) and 8(d)
ddinlist = [0:7];
RovRLlist = [0 1 2];

for mm = 1:length(RovRLlist)
    RovRL = RovRLlist(mm);
%    c1 = 1/(RovRL+1);  % For part (c), uncomment this line and comment the one below
    c1 = 1;             % For part (d), uncomment this line and comment the one above
    for kk = 1:length(ddinlist)
        binin = dec2bin(ddinlist(kk),3);
        vout(mm,kk) = c1*(str2num(binin(1))*0.5 + str2num(binin(2))*0.25 + str2num(binin(3))*0.125);
    end
end

figure; plot(ddinlist, vout,  '-o', 'LineWidth', 2);
grid on;
xlabel('Decimal input'); ylabel('Output voltage, v_{out} (V)' );
legend('R_L = \infty','R_L = R','R_L = R/2','Location','northwest');
ylim([0 1])
set(gcf,'Color',[1 1 1]); set(gcf, 'MenuBar','default');
```

```
% Boston University - EK307-A1
% Homework 5, Problem 8
% M. Popovic, Oct 8, 2017

clear all; close all;

vs = 1;             % Voltage of input sources when bit value is 1 (here 1V).  It is 0V for bit value 0.
N  = 3;             % Number of bits

% A. Find circuit response for each possible bit sequence from 000 to 111.

% A.1 Define binary input(s)
bveclist = [];              % Create a list of all bit sequences and run through them
for kk = 0:2^N-1            % Run through list of all N-bit numbers
    bbin = dec2bin(kk,N);   % Take each decimal number kk and get its binary form as a string
    % Put it into a row of the bveclist matrix
    for mm=1:length(bbin), bveclist(kk+1,mm) = str2double(bbin(mm));   end;
end

% A.2 Specify resistor list for the DAC
% Specify cct resistors [R1 R2 R3 R4 R5 R6] (e.g. in kiloohms); see figure.
% Rlistvec = [2 2 1 2 1 2];                  % For 3-bit DAC.
Rlistvec = [2 2 repmat([1 2],1,N-1)];          % General case for N-bit DAC

% A.3 Run through all possible N-bit inputs, get vout, and print it.
for kk = 0:2^N-1                               % Now cycle through all the inputs and solve
    bvec = bveclist(kk+1,:);                   % Set voltage sources for kk-th bit sequence
    vout(kk+1) = r2rdac(Rlistvec,bvec*vs);           % Solve circuit to get output voltage
    fprintf( 'For decimal input %02d (binary %s), vout = %g V\n'  ,kk,dec2bin(kk,N),vout(kk+1));
end

% A.4 Plot vout vs. decimal input
figure; plot(0:2^N-1, vout,  '-o', 'LineWidth', 2); ylim([0 1]*vs); grid  on;
xlabel( 'Decimal input' ); ylabel( 'Output voltage, v_{out} (V)' );
set(gcf,'Color',[1 1 1]); set(gcf, 'MenuBar','default');


% Function that solves N-bit R-2R DAC circuit, given resistors in
% vector Rlistvec = [R1 R2 R3 R4 R5 R6] (for 3-bit), and vin = [v2 v1 v0]
% input bit sequence as a 3 element numerical row vector (as a voltage).
function [vout,vnodes] = r2rdac(Rlistvec,vin)
    % B.1 Generate the node-voltage matrix and vector of constants representing the circuit
    D1 = -1./Rlistvec(3:2:end-1);              % For off-diagonal, take -1/R3, -1/R5, ...
    D2 = 1 ./ Rlistvec(1:2:end-1) +  ...       % For diagonal, take [1/R1,1/R3,...], ...
         1 ./ Rlistvec(2:2:end) +  ...         % and add [1/R2,1/R4,...], ...
         [1./Rlistvec(3:2:end-1), 0];          % finally add [1/R3,1/R5,...] except in the last element.

    A = diag(D2) + diag(D1,1) + diag(D1,-1);   % Create the matrix A from the above diagonals
    b = 1./Rlistvec(2:2:end).' .* fliplr(vin).';   % Create the right-hand side vector, b, for this input
    vnodes = A\b;                              % Solve for node voltages [V0prime, V1prime, V2prime,...]
    vout = vnodes(end);                        % Store the vout values in a vector
end
```

```
% Boston University - EK307-A1
% Homework 5, Problem 8
% M. Popovic, Oct 8, 2017

clear all; close all;

vs = 1;             % Voltage of input sources when bit value is 1 (here 1V).  It is 0V for bit value 0.
N  = 3;             % Number of bits

% A. Find circuit response for each possible bit sequence from 000 to 111.

% A.1 Define binary input(s)
bveclist = [];              % Create a list of all bit sequences and run through them
for kk = 0:2^N-1            % Run through list of all N-bit numbers
    bbin = dec2bin(kk,N);   % Take each decimal number kk and get its binary form as a string
    % Put it into a row of the bveclist matrix
    for mm=1:length(bbin), bveclist(kk+1,mm) = str2double(bbin(mm));   end;
end

% A.2 Specify resistor list for the DAC
% Specify cct resistors [R1 R2 R3 R4 R5 R6] (e.g. in kiloohms); see figure.
% For 3-bit DAC, we manually come up with a few cases of resistors off by
% 5%:
Rlistvec(1,:) = [2 2 1 2 1 2] .* [0.95 1.05 1.05 0.95 0.95 0.95];   % Case 1
Rlistvec(2,:) = [2 2 1 2 1 2] .* [1.05 1.05 0.95 0.95 0.95 1.05];
Rlistvec(3,:) = [2 2 1 2 1 2] .* [0.95 1.05 0.95 0.95 0.95 0.95];
Rlistvec(4,:) = [2 2 1 2 1 2] .* [0.95 1.05 0.95 1.05 0.95 1.05];
Rlistvec(5,:) = [2 2 1 2 1 2] .* [1.05 1.05 0.95 0.95 0.95 0.95];
Rlistvec(6,:) = [2 2 1 2 1 2] .* [1.05 1.05 1.05 0.95 0.95 0.95];   % Case 6

% A.3o Run through all 6 above practical circuit builds
for mm = 1:size(Rlistvec,1)
    % A.3 Run through all possible N-bit inputs, get vout, and print it.
    for kk = 0:2^N-1                                % Now cycle through all the inputs and solve
        bvec = bveclist(kk+1,:);                    % Set voltage sources for kk-th bit sequence
        vout(kk+1,mm) = r2rdac(Rlistvec(mm,:),bvec*vs);   % Solve circuit to get output voltage
        fprintf( 'For decimal input %02d (binary %s), vout = %g V\n'  ,kk,dec2bin(kk,N),vout(kk+1));
    end
end

% A.4 Plot vout vs. decimal input
figure; plot(0:2^N-1, vout,  '-o', 'LineWidth', 2); ylim([0 1]*vs); grid  on;
xlabel( 'Decimal input' ); ylabel( 'Output voltage, v_{out} (V)' );
set(gcf,'Color',[1 1 1]); set(gcf, 'MenuBar','default');


% Function that solves N-bit R-2R DAC circuit, given resistors in
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    % B.1 Generate the node-voltage matrix and vector of constants representing the circuit
    D1 = -1./Rlistvec(3:2:end-1);               % For off-diagonal, take -1/R3, -1/R5, ...
    D2 = 1 ./ Rlistvec(1:2:end-1) +  ...        % For diagonal, take [1/R1,1/R3,...], ...
         1 ./ Rlistvec(2:2:end) +  ...          % and add [1/R2,1/R4,...], ...
         [1./Rlistvec(3:2:end-1), 0];           % finally add [1/R3,1/R5,...] except in the last element.

    A = diag(D2) + diag(D1,1) + diag(D1,-1);    % Create the matrix A from the above diagonals
    b = 1./Rlistvec(2:2:end).' .* fliplr(vin).';    % Create the right-hand side vector, b, for this input
    vnodes = A\b;                               % Solve for node voltages [V0prime, V1prime, V2prime,...]
    vout = vnodes(end);                         % Store the vout values in a vector
end
```