BOSTON UNIVERSITY

EK 307: Electric Circuits

Fall 2017

Lecture 12

Oct 19, 2017

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Boston University

Administrivia

- Homework 5 due today
  - Problem 8: can hand in next week with HW6.

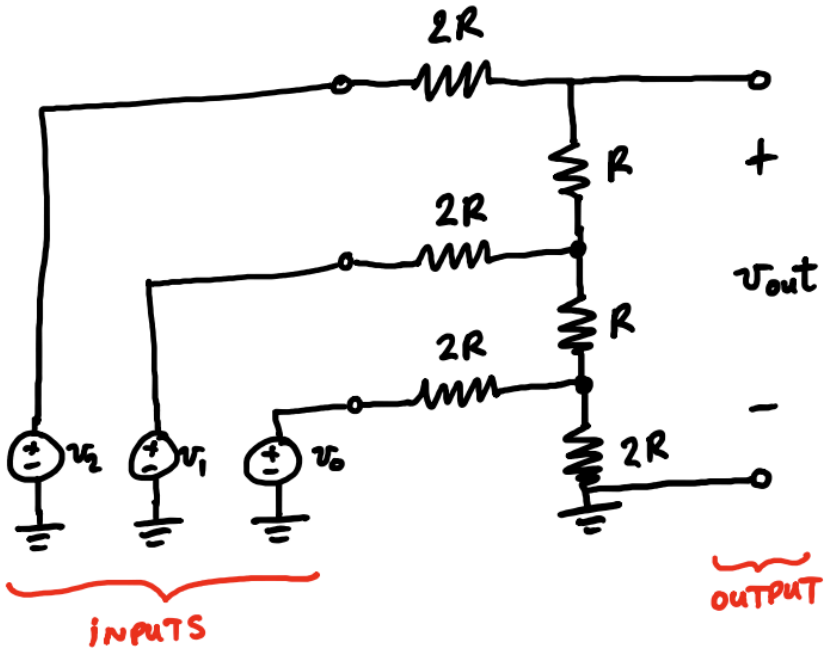
- Midterm Exam #1 discussion

Problem 8. [Revision 2]. (Part 2; continued from Problem Set 4 – Problem 10)

Design problem: toward a digital-to-analog converter (DAC).

In the last problem set, you looked at the Thevenin equivalent of the 3-bit R-2R DAC with respect to each of the three bit input voltages (v_0, v_1, v_2), and you showed the output voltage for an arbitrary analog set of input voltages and for all 3-bit digital input combinations at (v_0, v_1, v_2) using 1V sources.

This week, we want to understand how this DAC design behaves and whether it works (1) when you connect a resistive load to it, and (2) to develop a short Matlab code that can let you quickly analyze the circuit with arbitrary choice of resistance values for the 6 resistors, and show that it works. Then, test how the DAC performs if your resistors are off by 5% from their target values (fabrication tolerance) in a few different ways you choose.



(a) Give a single equation that gives the output voltage, v_{out}, as a function of the three (v_0, v_1, v_2) input voltages. Use the superposition principle to do this.

(b) Find v_{out} when you connect an arbitrary load resistor R_L to the DAC output. Give the single equation, just like in part (a). Hint: you can look at the Thevenin equivalents you found in the last homework, with the load connected to it, and use superposition.

(f) Put your matrix equation into Matlab, and write a function that returns v_{out} given inputs (v_0,v_1,v_2). Then, write a script that sets R_1 to R_6 to the circuit from Homework 4 Prob 10, with R = 1kΩ, (i.e. 1kΩ and 2kΩ resistors) and run it through the 8 bit combinations to produce the same plot you got by hand in Homework 4. Show the plot from Matlab, and the code. Keep the code as short and compact as possible.

(g) Set the resistors (R_1 to R_6) using resistor values that are 5% off the target value, i.e. use R = 0.95kΩ or 1.05kΩ instead of 1kΩ. For each of the 6 resistors pick randomly whether the resistor is 5% too high or low. Use your Matlab code to plot the output voltage vs. 0 to 7 digital input for three cases (ie choose the 6 resistors randomly – or it doesn't have to be random – choose them in some combination you wish – three times). Show those 3 curves on top of the line for the ideal case from part (d) with R_L = infinity.

Keep your code. We will use it in next week's problem set.

Lecture 11: Last time

1. **Review opamp**
2. **Cascading Op Amps (continued)**
3. **Summing amplifiers**
4. **Differencing amplifiers**
5. **Applications: instrumentation amp**

Lecture 12: Today

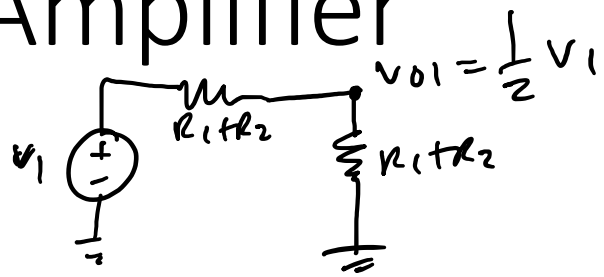
1. **Review of midterm exam**
2. **Applications: DAC, instrumentation amp**
3. **DAC on the homework**

Next time:

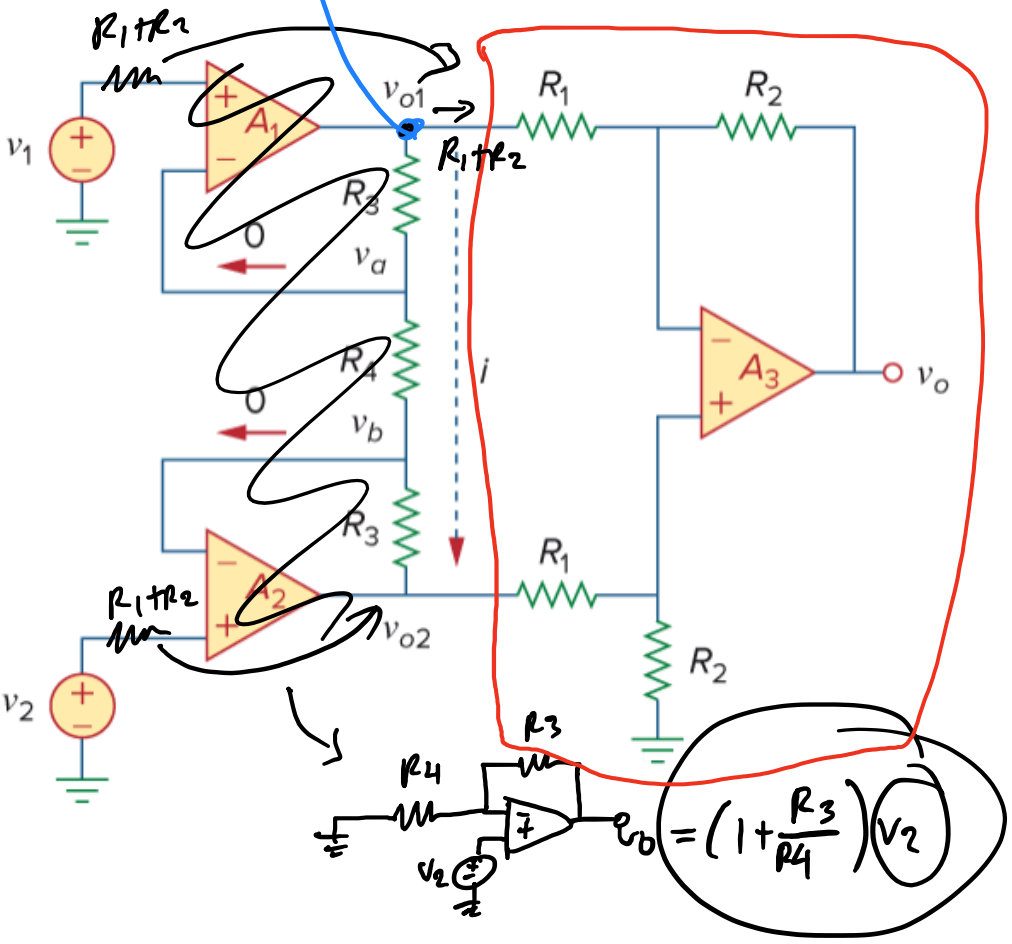
1. **Chapter 6: Capacitors/inductors**

Review of Midterm Exam 1

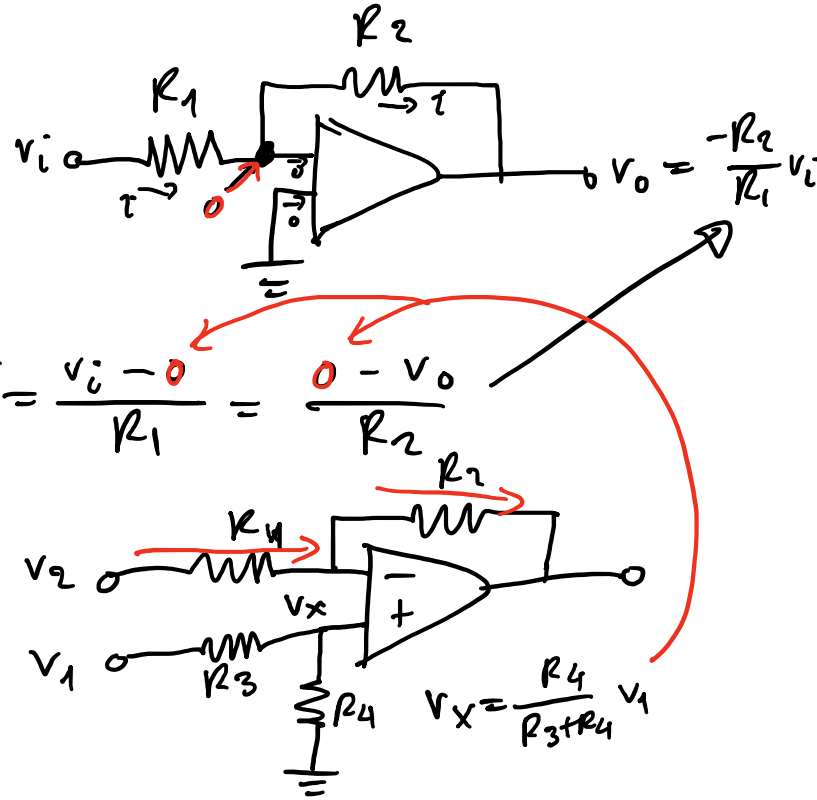
Instrumentation Amplifier

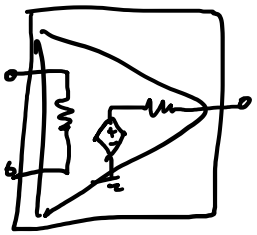


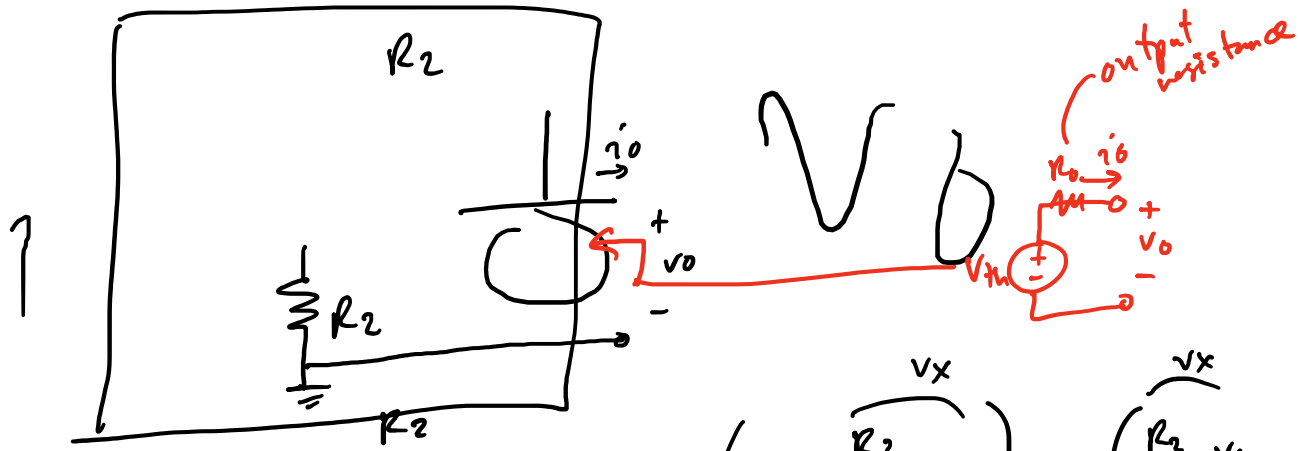
Show that: $v_o = \frac{R_2}{R_1}\left(1 + \frac{2R_3}{R_4}\right)(v_2 - v_1)$

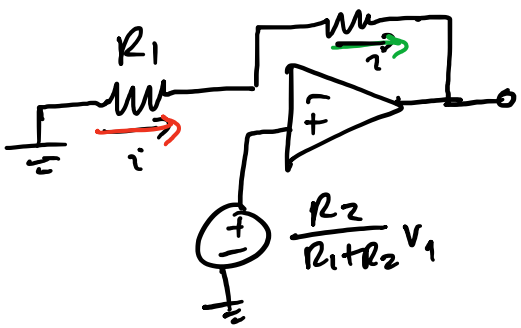


Discussion: what does this do?

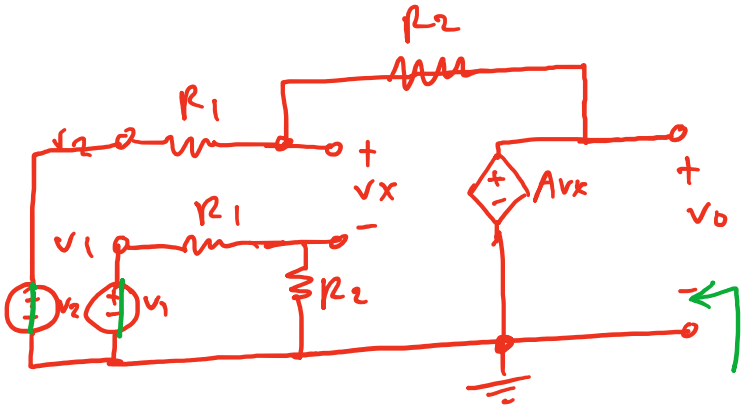








$$i = \frac{\left(0 - \overbrace{\frac{R_2}{R_1+R_2}v_1}^{v_x}\right)}{R_1} = \frac{\left(\overbrace{\frac{R_2}{R_1+R_2}v_1}^{v_x} - v_0\right)}{R_2}$$

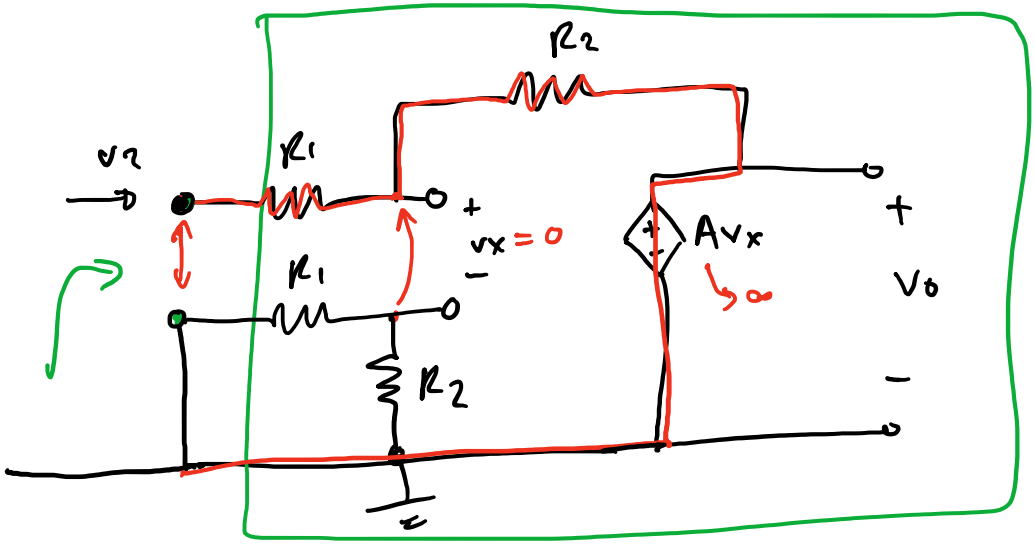


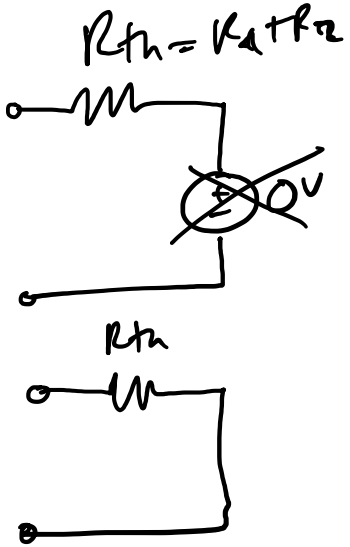
$$-\frac{R_2}{R_1}v_x = v_x - v_0$$

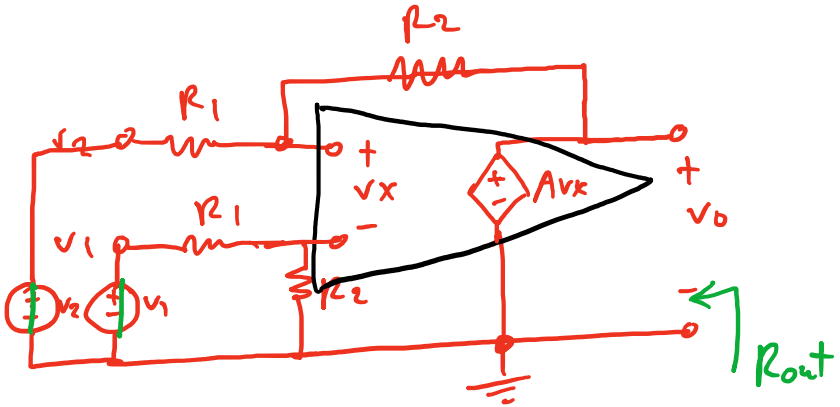
$$v_0 = \left(1 + \frac{R_2}{R_1}\right)v_x$$

$$= \left(\frac{R_1+R_2}{R_1}\right)\frac{R_2}{R_1+R_2}v_1$$

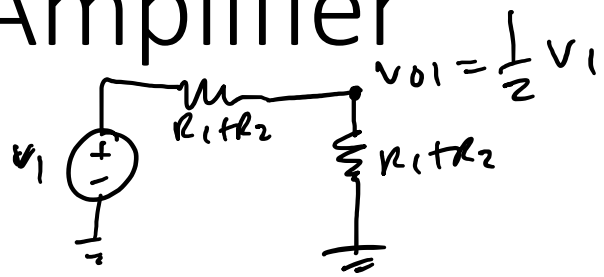
$$= \frac{R_2}{R_1}v_1$$


R2
R1
V2
+
vx = 0
−
R1
R2
Avx
∞
+
Vo
−


Rth = R1 + R2
0V
Rth

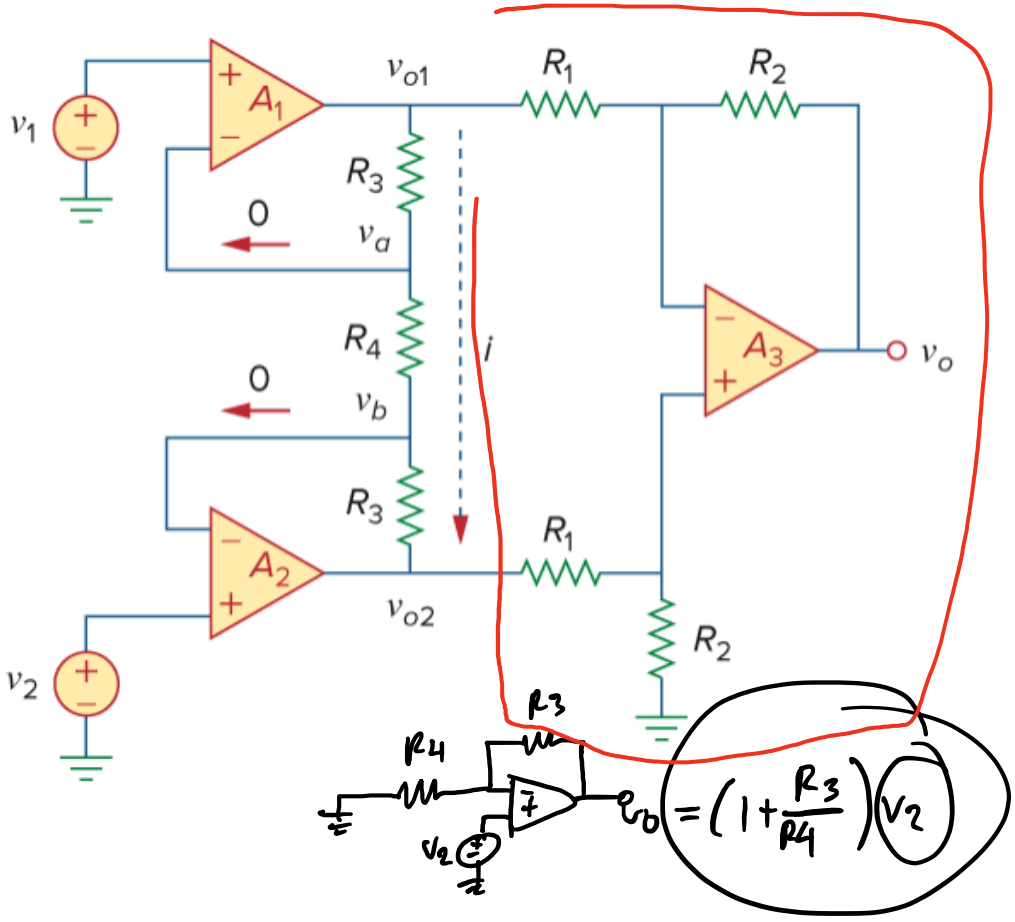

R2
R1
V2
+
vx
−
R1
V1
Avx
+
Vo
V2
V1
R2
Rout

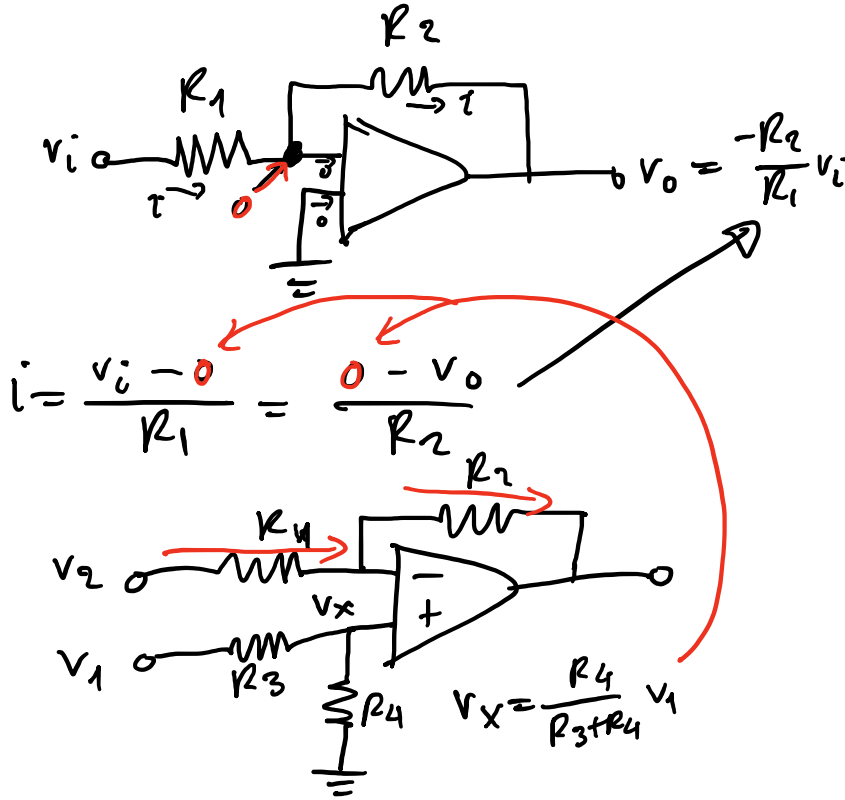
Instrumentation Amplifier



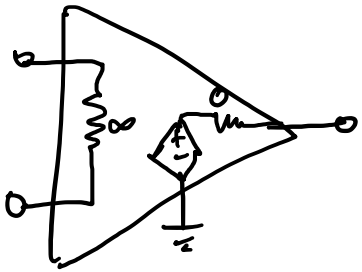
Show that: $v_o = \frac{R_2}{R_1}\left(1 + \frac{2R_3}{R_4}\right)(v_2 - v_1)$

Discussion: what does this do?



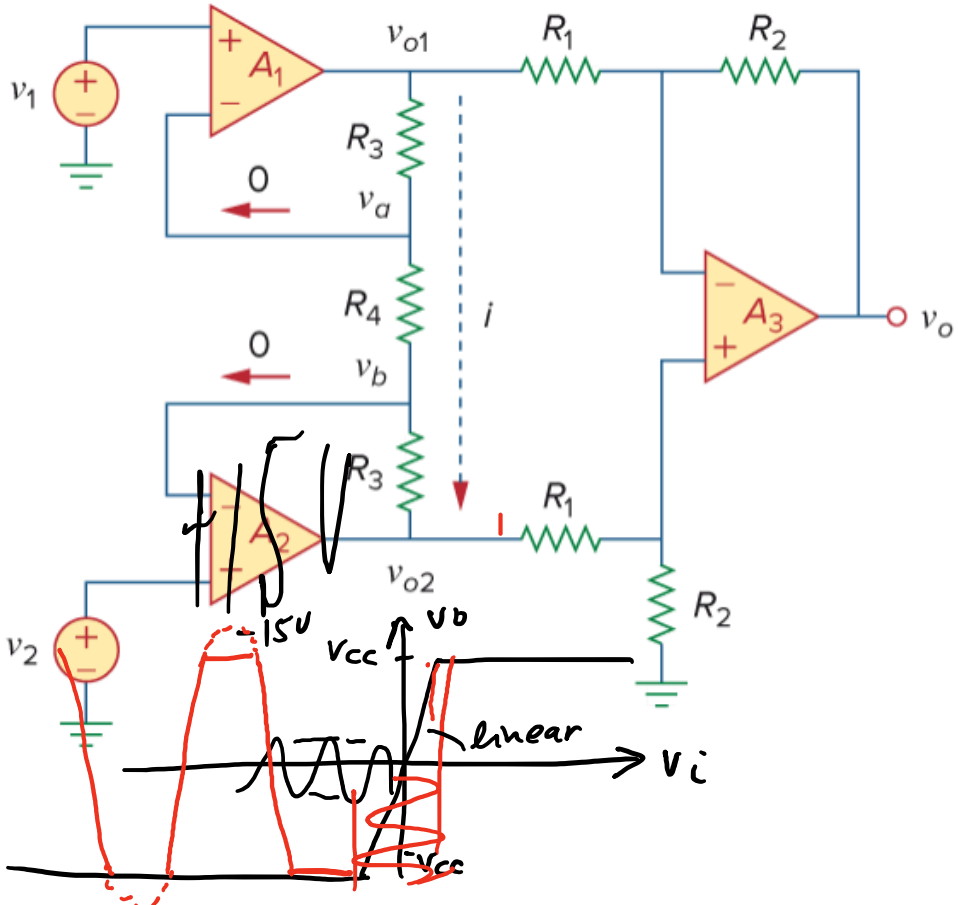


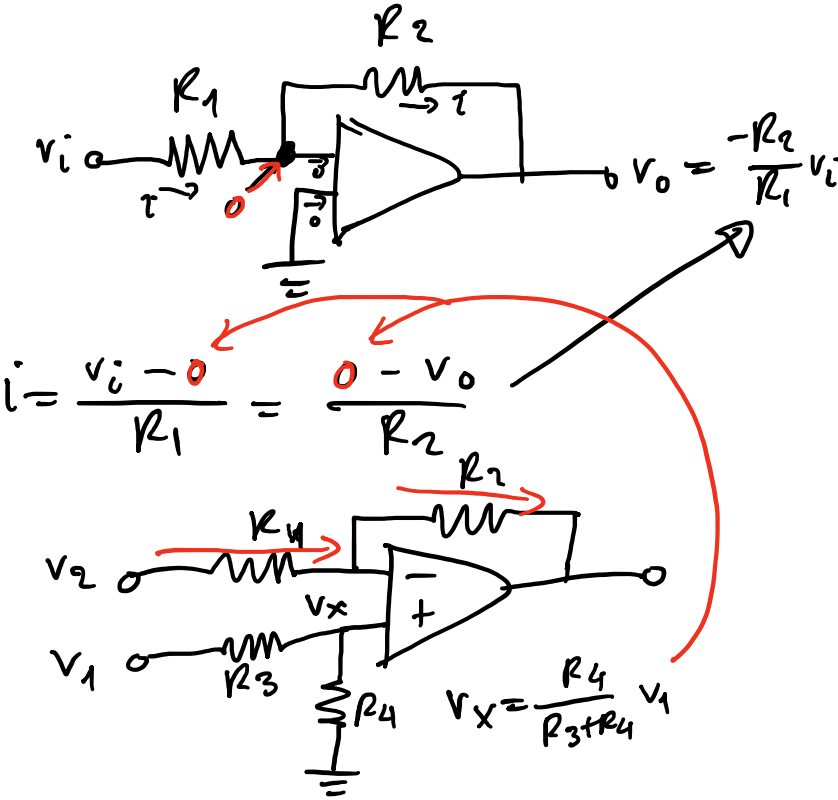
Instrumentation Amplifier



Show that: $$v_o = \frac{R_2}{R_1}\left(1 + \frac{2R_3}{R_4}\right)(v_2 - v_1)$$

Discussion: what does this do?





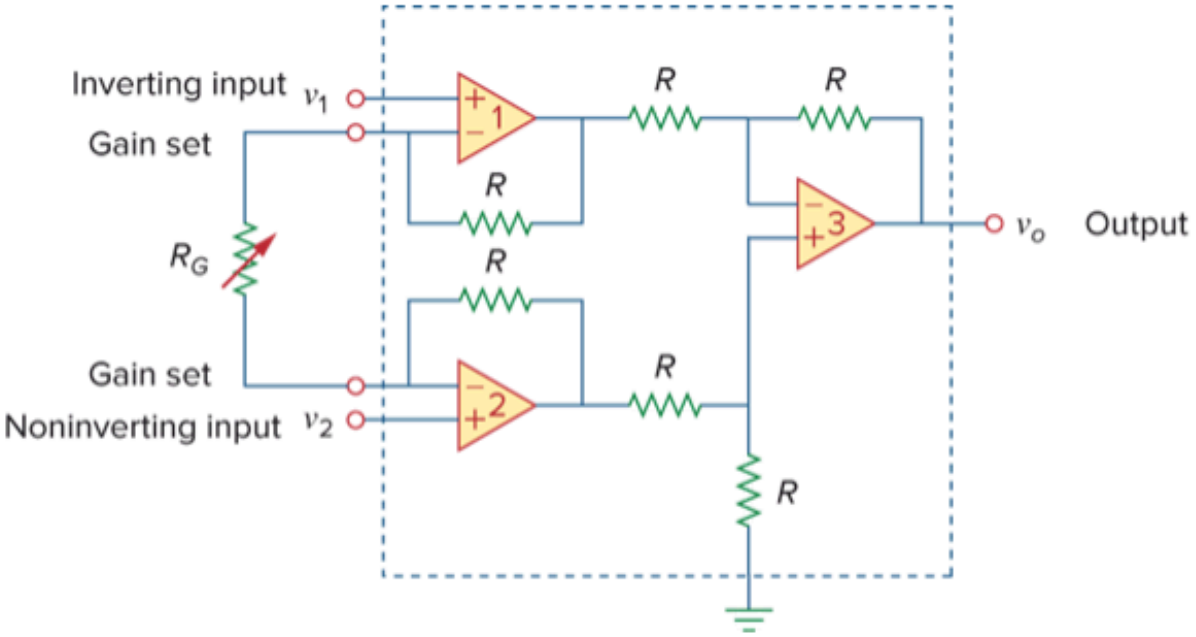
Instrumentation Amplifier

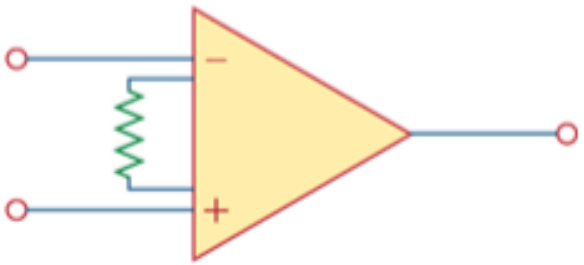
Now that we talked about it, check out:
https://en.wikipedia.org/wiki/Instrumentation_amplifier

Instrumentation Amplifiers

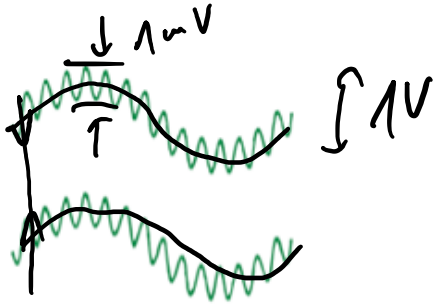
$$v_o = A_v(v_2 - v_1)$$

$$A_v = 1 + \frac{2R}{R_G}$$

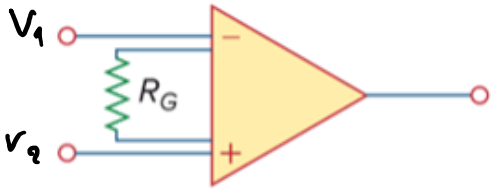




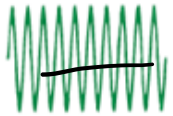
Instrumentation Amplifiers



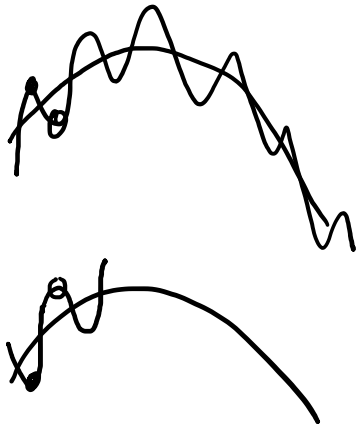
Small differential signals riding on larger common-mode signals



Instrumentation amplifier



Amplified differential signal, no common-mode signal



Example application: optical receivers

A 12Gb/s, 8.6μA$_{pp}$ Input Sensitivity, Monolithic-Integrated Fully Differential Optical Receiver in CMOS 45nm SOI process

Nandish Mehta[1], Chen Sun[1], Mark Wade[2], Sen Lin[1], Milos Popović[2] and Vladimir Stojanović[1]
[1]University of California Berkeley, CA, USA and [2]University of Colorado Boulder, CO, USA
nandish@berkeley.edu

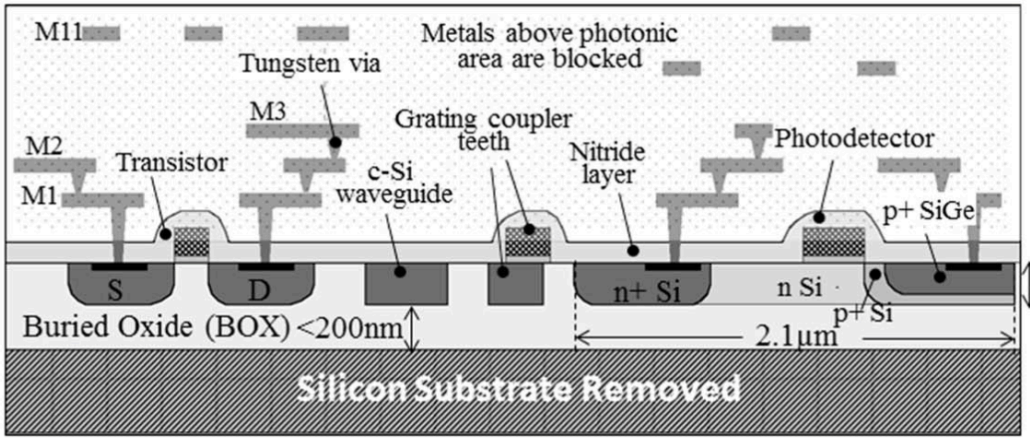
***Abstract*— A high-sensitivity, fully-differential optical receiver for high-density photonic interconnects is presented. To realize fully-differential operation, a 3-dB power splitter and SiGe photodetector are integrated with the receiver, all in a CMOS 45nm SOI process. The proposed receiver improves sensitivity by suppressing common-mode and supply noise through fully-differential (FD) operation, achieving 12Gb/s at BER <10^{-12} with input sensitivity of 8.6μA$_{PP}$ while consuming 4.3mW. To understand the effectiveness of the proposed solution, we compare it to a conventional single-ended (SE) receiver on the same test-chip. Measured sensitivity is >2x better than the closest state-of-the-art design, achieving same energy per bit at higher data-rate.**

TABLE I. PERFORMANCE AND LOSS OF OPTICAL SUB-BLOCKS AT λ=1180nm

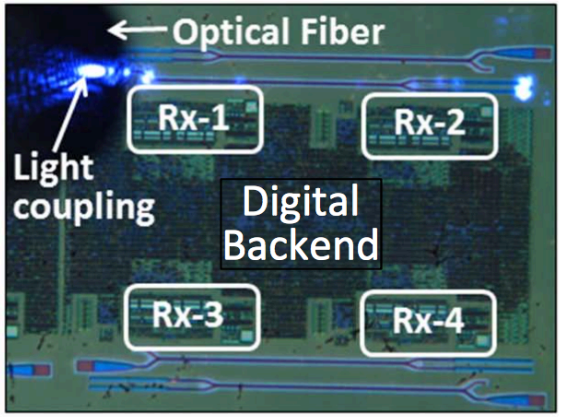
Block	Parameter	Measured	Best Device[a]
Grating-Coupler	Coupling Loss	4.4dB	1.2dB
Waveguide	Insertion Loss	4.3dB/cm	4.3dB/cm
Photodetector	Responsivity, R	0.023A/W	0.55A/W
	Bandwidth	5GHz	~3.3 GHz

[a.] Measured from standalone devices on recent photonic-only chips or this test-chip.

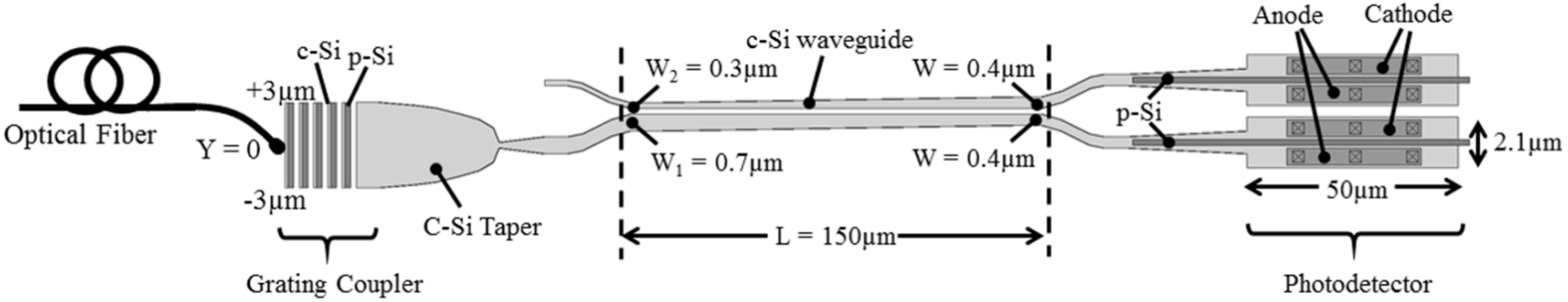
In this work, we present three design techniques for improving receiver sensitivity. First, taking advantage of the low parasitics of the single-chip electro-optic platform, a high-gain (and thus,



(a) Cross-section of electro-optic platform



(b) Micrograph of 1 of the 3 test-sites



(c) Integrated 3dB power splitter and SiGe Photodetector

Fig. 1. Single Chip Electro-Optic platform in CMOS 45nm SOI Process.

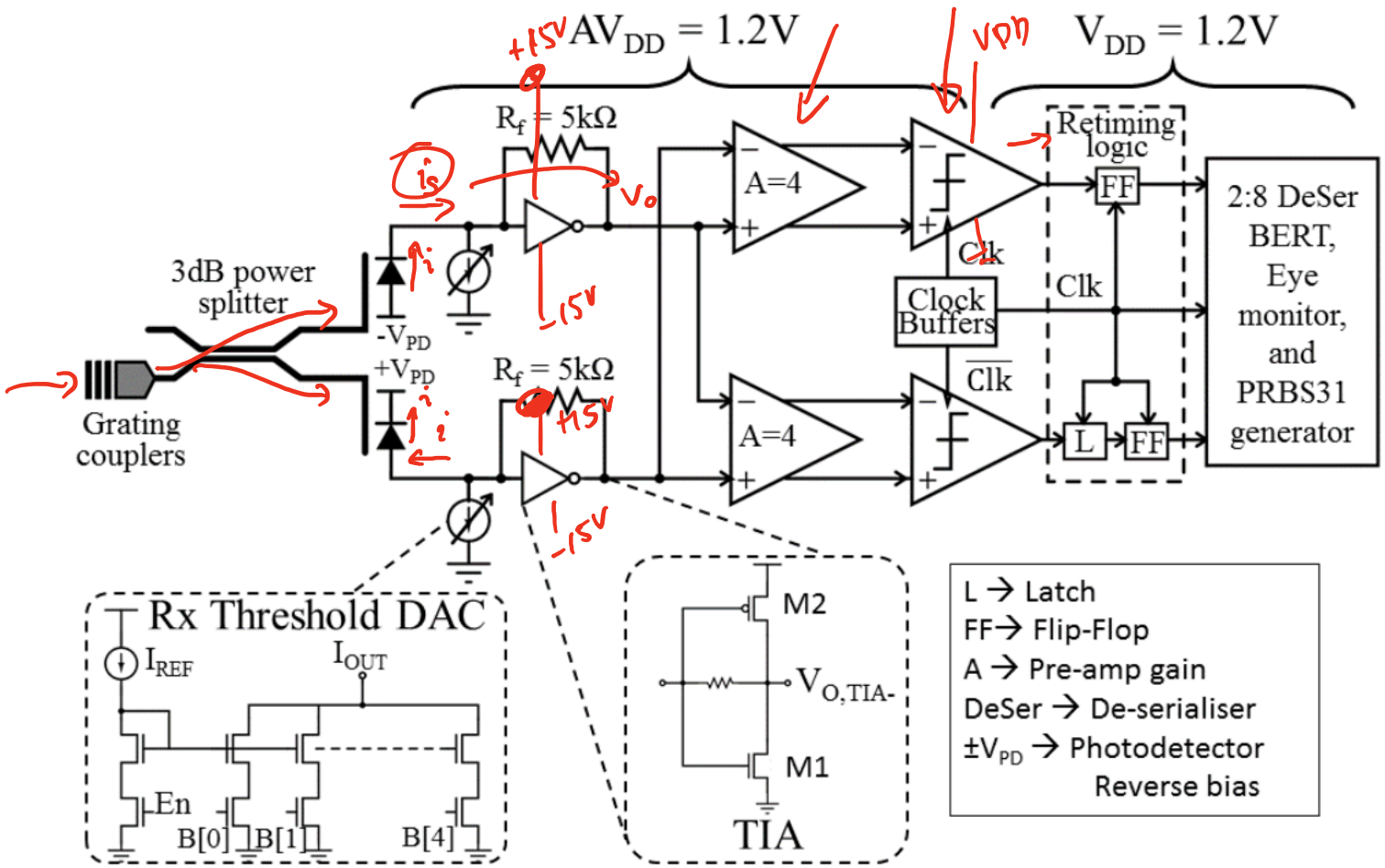
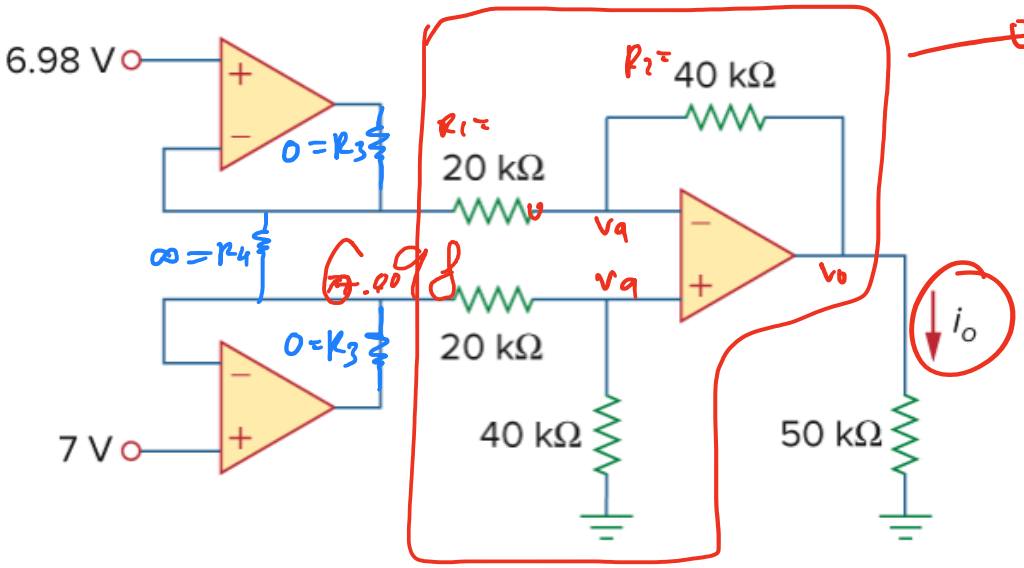


Fig. 2. Block diagram of proposed fully-differential optical receiver

Example

Obtain i_o in the instrumentation amplifier circuit of Fig. 5.27.



Differential amplifier:

$$v_o = \frac{-R_2}{R_1}(v_2 - v_1)$$

$$\frac{v_2 - v_a}{20k} = \frac{v_a - v_o}{}$$

$$\frac{v_1 - v_a}{20k} = v_a$$

$$v_o = \frac{-40k}{20k}(-0.02) = 0.04\ V$$

$$i_o = \frac{0.04V}{50k\Omega} = \frac{40\ mV}{50\ k\Omega} = 0.8\ \mu A$$

Figure 5.27 Instrumentation amplifier; for Practice Prob. 5.8.

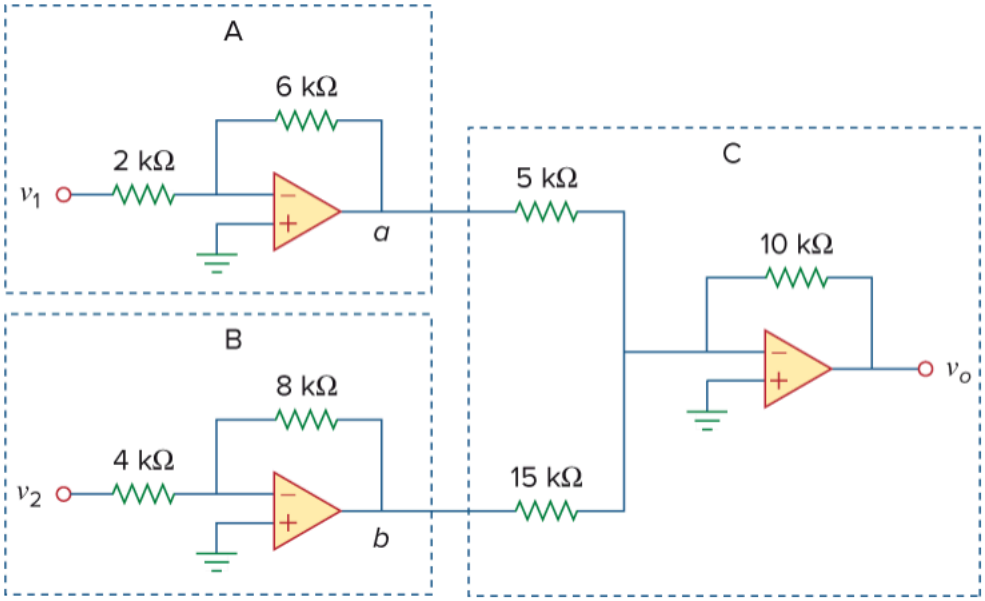
Instrumentation amp:

$$V_o = \frac{-R_2}{R_1}\left(1 + \frac{2R_3}{R_4}\right)(v_2 - v_1)$$

($R_3 \to 0$, $R_4 \to \infty$)

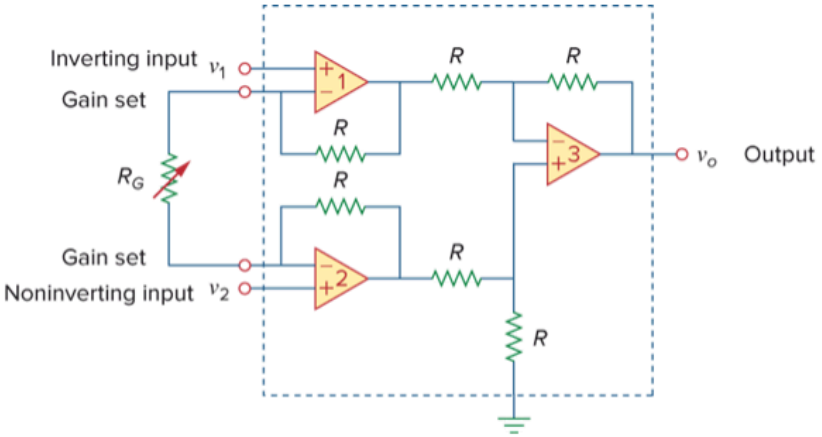
Example (students)

If $v_1 = 1$ V and $v_2 = 2$ V, find v_o in the op amp circuit of **Fig. 5.31**.



Example (students)

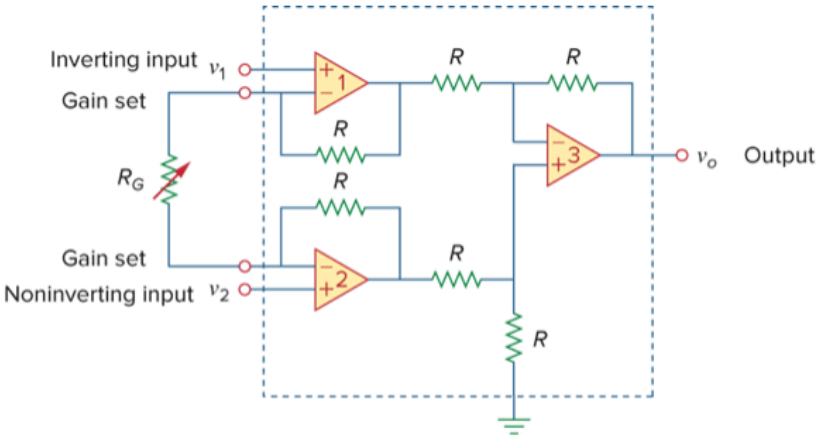
$$v_o = A_v(v_2 - v_1)$$



In **Fig. 5.38**, let $R = 10\ \text{k}\Omega$, $v_1 = 2.011$ V, and $v_2 = 2.017$ V. If R_G is adjusted to 500 Ω, determine: (a) the voltage gain, (b) the output voltage v_o.

Example (students)

$$v_o = A_v(v_2 - v_1)$$



In **Fig. 5.38**, let $R = 10\ \text{k}\Omega$, $v_1 = 2.011$ V, and $v_2 = 2.017$ V. If R_G is adjusted to 500 Ω, determine: (a) the voltage gain, (b) the output voltage v_o.

Solution:

(a) The voltage gain is

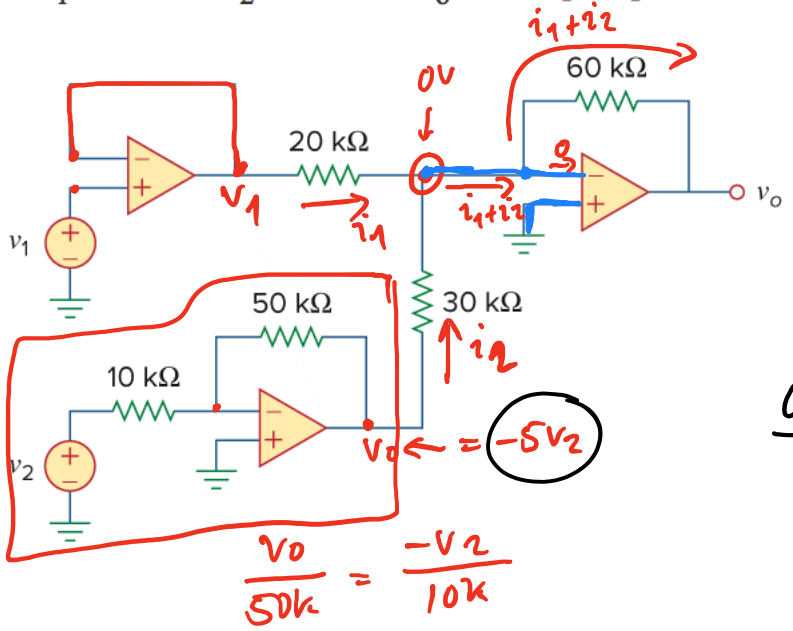
$$A_v = 1 + \frac{2R}{R_G} = 1 + \frac{2 \times 10{,}000}{500} = 41$$

(b) The output voltage is

$$v_o = A_v(v_2 - v_1) = 41(2.017 - 2.011) = 41(6)\ \text{mV} = 246\ \text{mV}$$

Example

If $v_1 = 5$ V and $v_2 = 5$ V, find v_o in the op amp circuit of Fig. 5.33.



– superposition voltage divider

$$\frac{v_1}{20k\Omega} = i_1 \quad , \quad \frac{-5v_2}{30k\Omega} = i_2$$

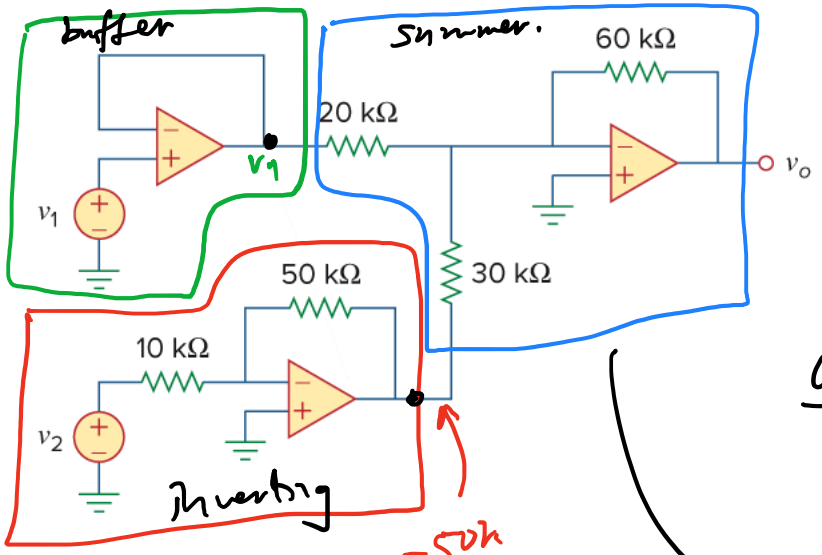
$$\frac{0 - v_o}{60k\Omega} = i_1 + i_2 = \frac{v_1}{20k} + \frac{-5v_2}{30k}$$

$$\frac{v_o}{50k} = \frac{-v_2}{10k}$$

$$\frac{v_o}{v_2} = \frac{-50}{10} = -5$$

Example

If $v_1 = 5$ V and $v_2 = 5$ V, find v_o in the op amp circuit of Fig. 5.33.

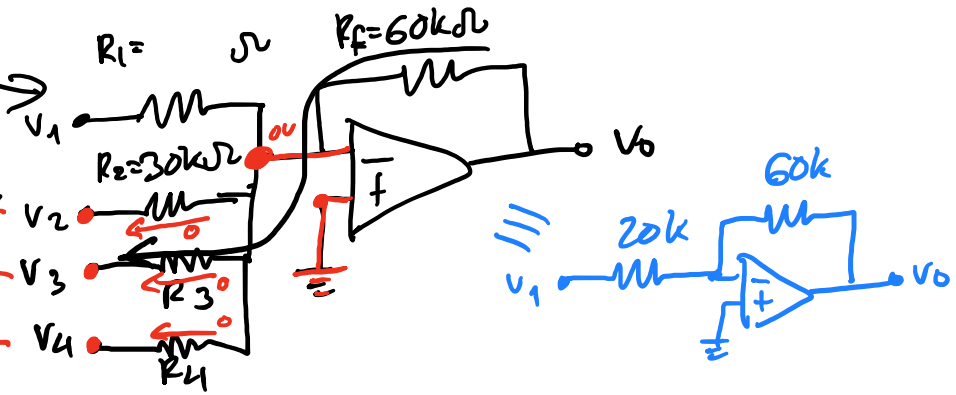


-superposition voltage divider

$$\frac{v_1}{20k\Omega} = i_1 \quad , \quad \frac{-5v_2}{30k\Omega} = i_2$$

$$\frac{0 - v_o}{60k\Omega} = i_1 + i_2 = \frac{v_1}{20k} + \frac{-5v_2}{30k}$$

$-\frac{50k}{10k} v_2$



$$v_o = -\left(\frac{R_f}{R_1} v_1 + \frac{R_f}{R_2} v_2 + \frac{R_f}{R_3} v_3 + \frac{R_f}{R_4} v_4\right)$$

Applications

Digital-to-Analog Converter

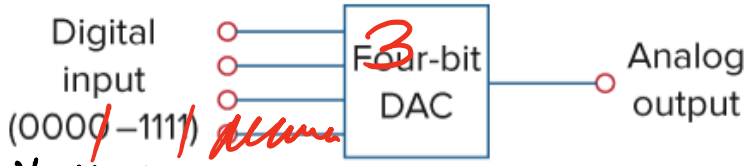
- Binary data…

https://www.youtube.com/watch?v=CTjolEUj00g

https://www.youtube.com/watch?v=B1BdQcJ2ZYY

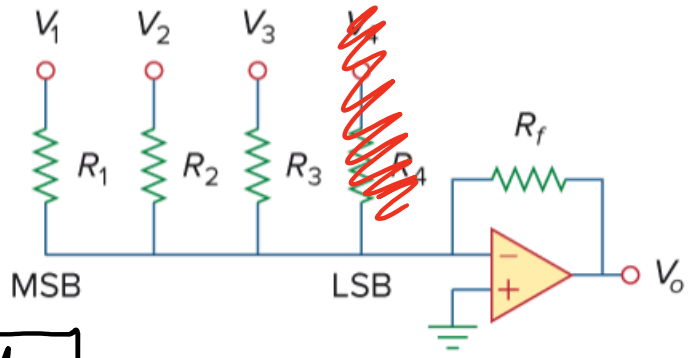
Digital-to-Analog Converter

$$-V_o = \frac{R_f}{R_1}V_1 + \frac{R_f}{R_2}V_2 + \frac{R_f}{R_3}V_3 + \frac{R_f}{R_4}V_4$$



V_1	V_2	V_3	
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

MSB LSB

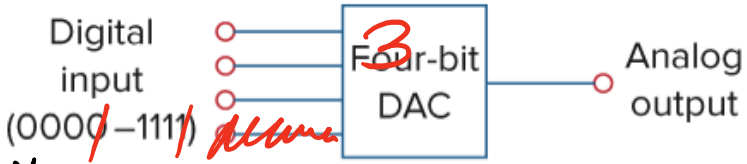


$$V_o = 4V_1 + 2V_2 + 1V_3$$

$$V_o = 8V_1 + 4V_2 + 2V_3 + 1V_4$$

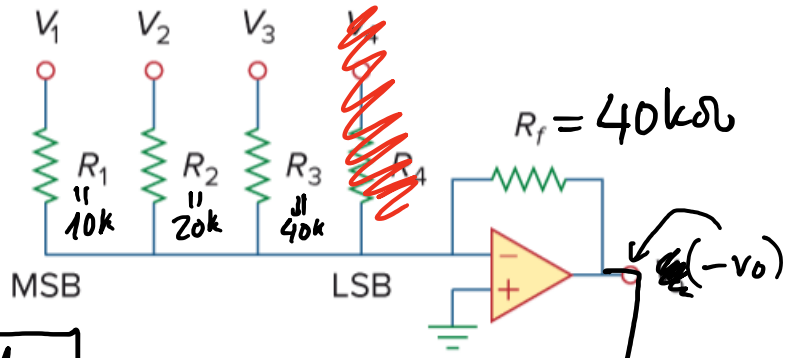
Digital-to-Analog Converter

$$-V_o = \frac{R_f}{R_1}V_1 + \frac{R_f}{R_2}V_2 + \frac{R_f}{R_3}V_3 + \frac{R_f}{R_4}V_4$$



V_1	V_2	V_3	
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

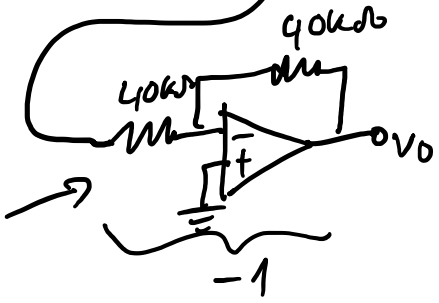
MSB ↗ ↖ LSB



$$V_o = 4V_1 + 2V_2 + 1V_3$$

$$V_o = -\left(-\left[\frac{R_f}{R_1}V_1 + \frac{R_f}{R_2}V_2 + \frac{R_f}{R_3}V_3\right]\right)$$

$+$ 4 2 1



Example (students)

A three-bit DAC is shown in **Fig. 5.37**.

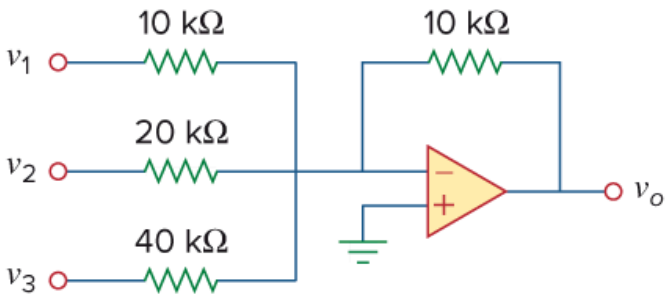


Figure 5.37 Three-bit DAC; for **Practice Prob. 5.12**.

(a) Determine $|V_o|$ for $[V_1 V_2 V_3] = [010]$.

(b) Find $|V_o|$ if $[V_1 V_2 V_3] = [110]$.

(c) If $|V_o| = 1.25$ V is desired, what should be $[V_1 V_2 V_3]$?

(d) To get $|V_o| = 1.75$ V, what should be $[V_1 V_2 V_3]$?

Example (students)

A three-bit DAC is shown in **Fig. 5.37**.

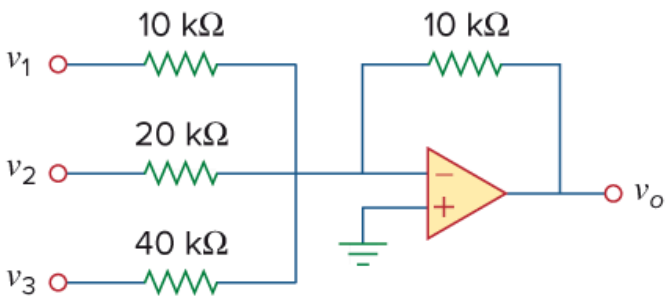


Figure 5.37 Three-bit DAC; for **Practice Prob. 5.12**.

(a) Determine $|V_o|$ for $[V_1V_2V_3] = [010]$.

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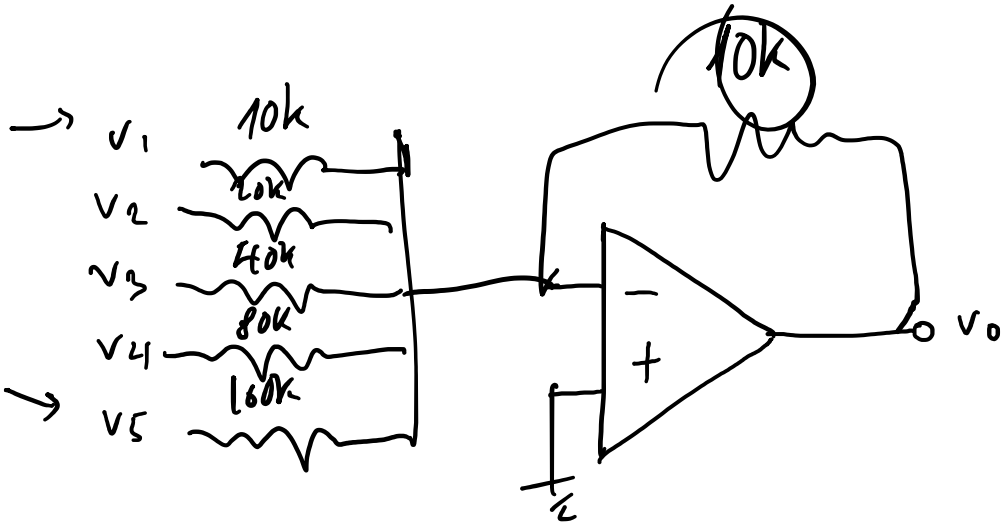
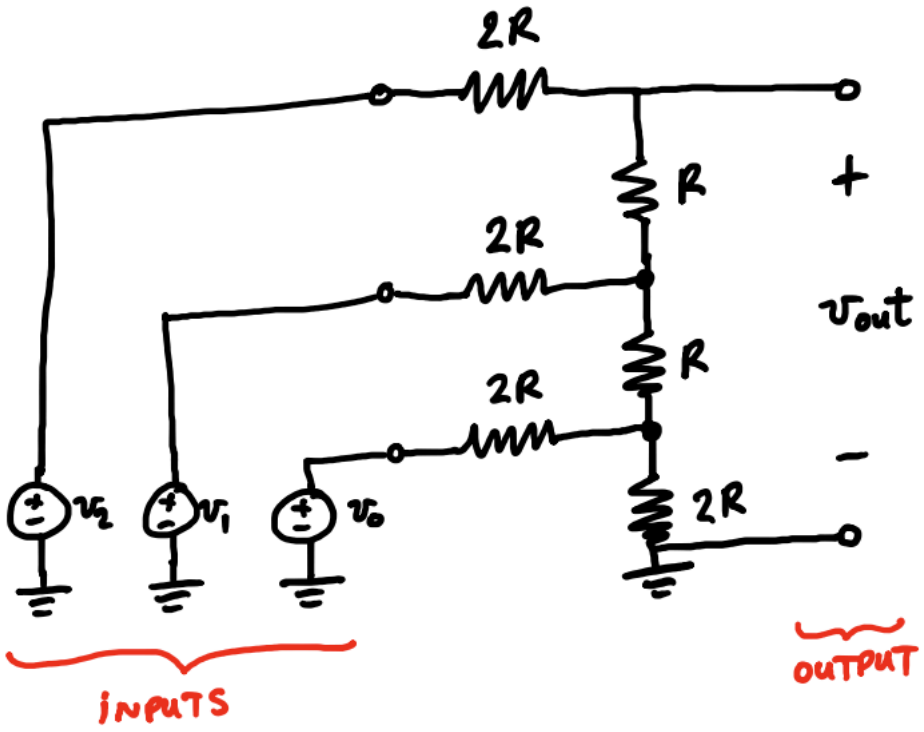
Answer: 0.5 V, 1.5 V, [101], [111].

Example: design a 5-bit DAC (students)



Homework #4 DAC Problem

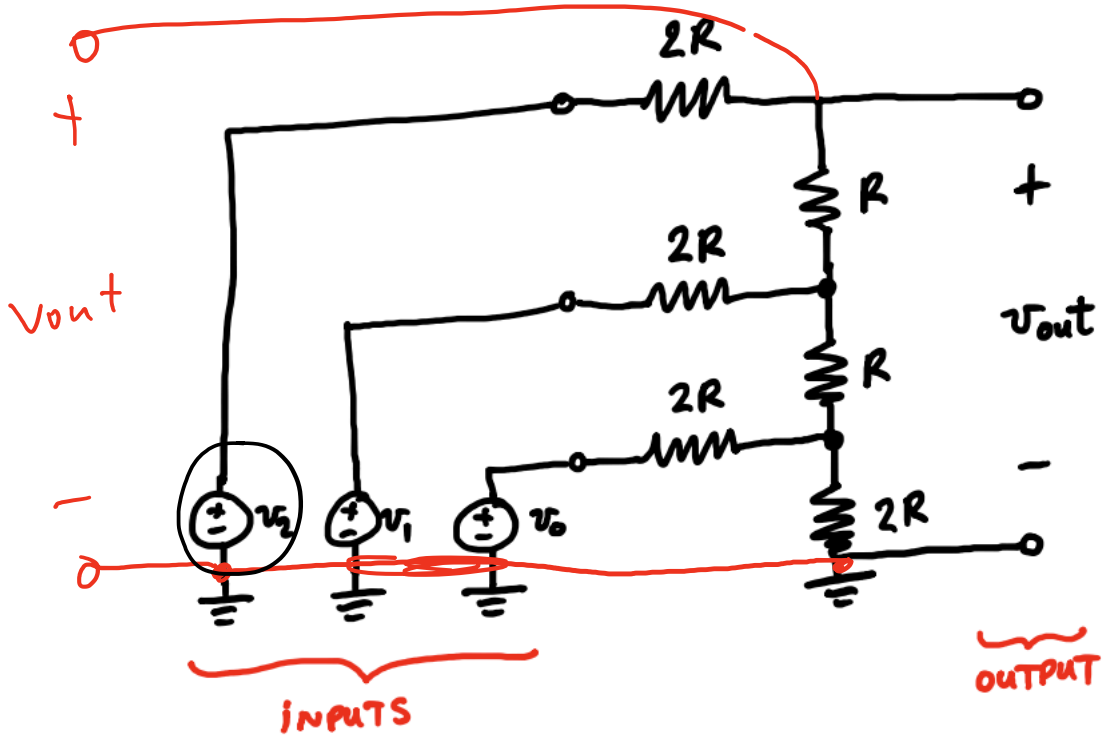


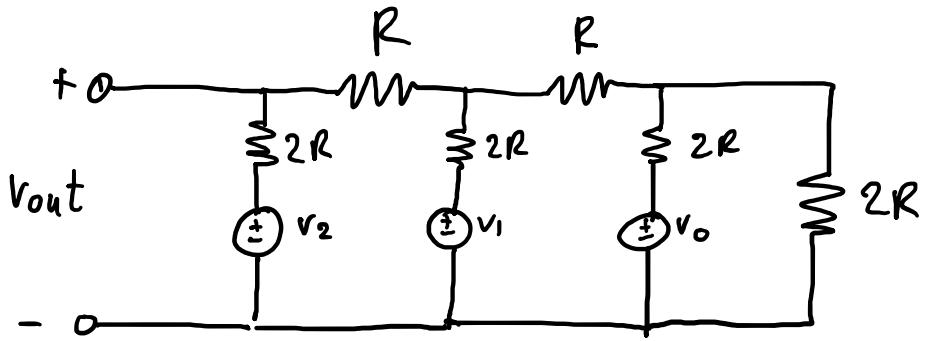
(a) Find the Thevenin equivalent with respect to the output terminals (v_{out}) for the circuit having two of the three voltage sources set to 0V (short). Provide the Thevenin equivalent circuit diagram and the transfer function v_{out}/v_n for each of n = 0, 1 and 2, with the other two sources turned off (i.e. one source at a time).

(b) Using superposition, what is v_{out} if $v_0 = 1V$, $v_1 = 2V$ and $v_3 = 3V$?

(c) To use the circuit as a DAC, all three voltage sources have values of only 1V or 0V to represent 1 or 0. Find v_{out} for (v_2, v_1, v_0) = (0,0,0), (0,0,1), (0,1,0), (0,1,1), (1,0,0), (1,0,1), (1,1,0),(1,1,1). Plot vout on the y axis vs the corresponding decimal value of these 3-bit numbers on the x-axis.

(d) Can you think on any drawbacks of this design?

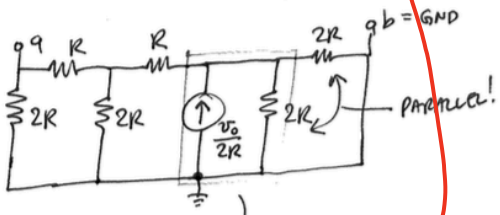

2R
R
2R
R
2R
2R
+
Vout
−
v_{out}
v_2
v_1
v_0
INPUTS
OUTPUT

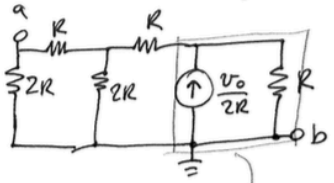

R
R
+
2R
2R
2R
2R
Vout
v_2
v_1
v_0
−

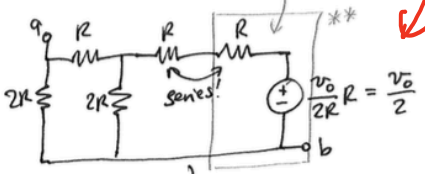
(10) (a) FOR v_o:

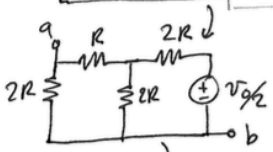
Thevenin: (find V_{oc} and R_{th})

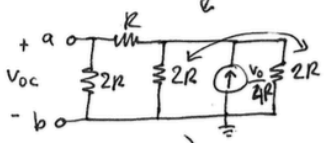
Use source transformations!

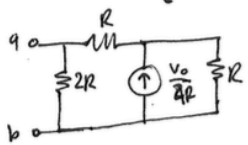


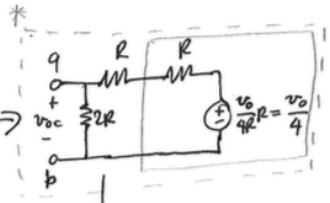


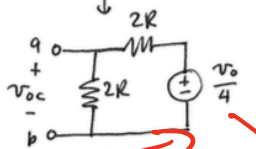


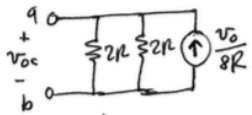


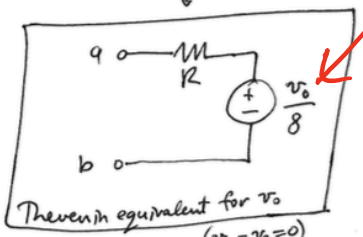






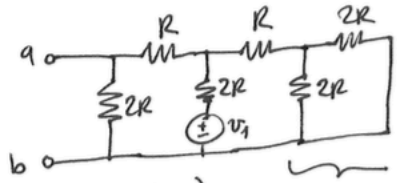


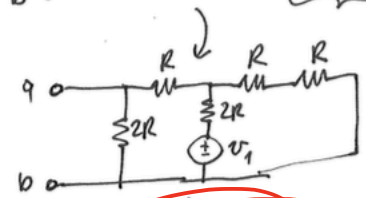


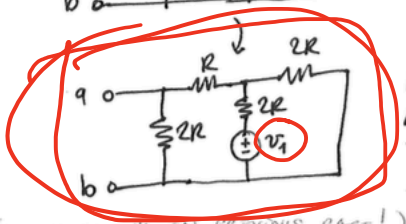


(CONT'D)

FOR v_1:



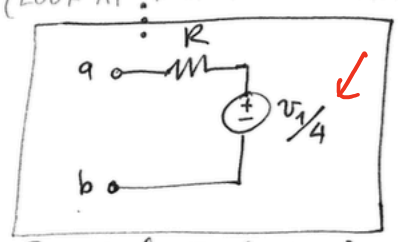




NOTE! NOTE THAT THIS IS EXACTLY THE SAME AS THE CCT FOR v_0 BUT WITH ONE LESS

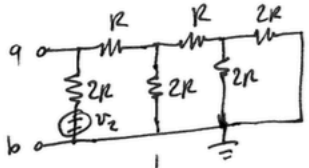
LADDER PART BEFORE THE TERMINALS.

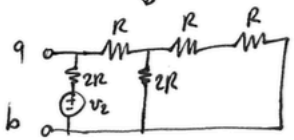
SO (LOOK AT * ON PREVIOUS PAGE!)

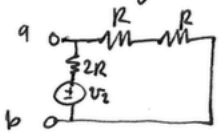


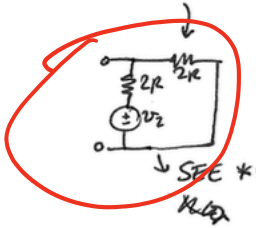
Thevenin for v_1 ($v_0 = v_2 = 0$)

For v_2 :

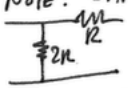




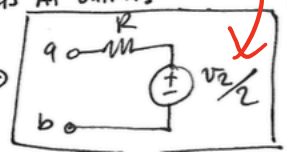




NOTE! SAME CCT AS FOR v_o BUT ~~[illegible]~~ WITHOUT TWO LADDER PARTS AT OUTPUT!



↓ SEE ** ON LAST PAGE!



Thevenin for v_2 ($v_o = v_1 = 0$)

(10) b) By superposition, with no load, for v_0, v_1 AND v_2 all non-zero,

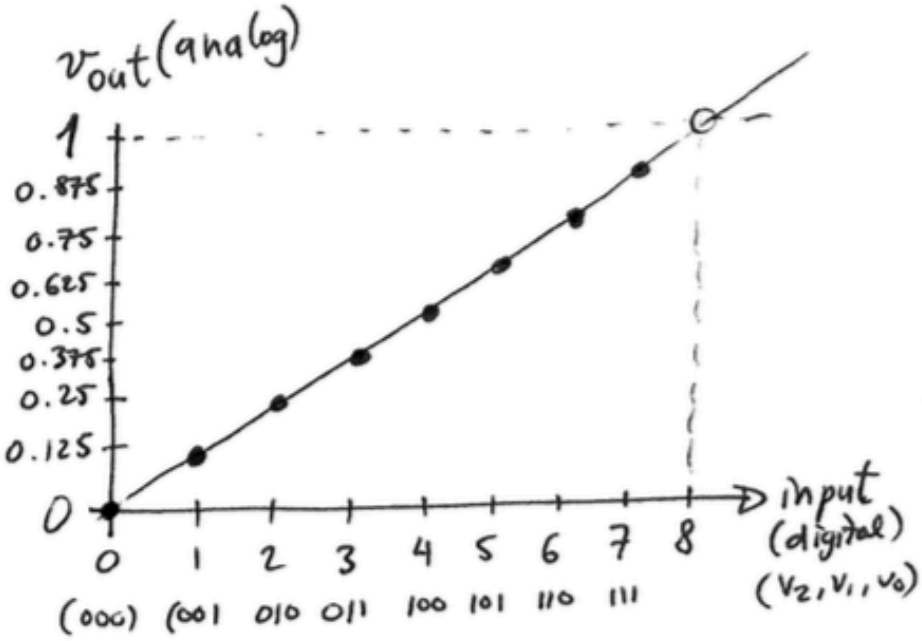
$$v_{out} = \frac{v_0}{8} + \frac{v_1}{4} + \frac{v_2}{2} \; !$$

If $v_0 = 1V$, $v_2 = 2V$, $v_3 = 3V$

$$v_{out} = \frac{1}{8} + \frac{2}{4} + \frac{3}{2} = \frac{1}{8} + \frac{1}{2} + \frac{3}{2} = 2.125\ V$$

c)

V_2	V_1	V_0	v_{out} (V)
0	0	0	0
0	0	1	0.125
0	1	0	0.25
0	1	1	0.375
1	0	0	0.5
1	0	1	0.625
1	1	0	0.75
1	1	1	0.875



Which is better?

Resistors only or op-amp version?

Discussion…