EC410 Lab #6 – Spring 2008

Project 1 –Current-Voltage Characteristics of the Bipolar Junction Transistor (Two Weeks)

BACKGROUND

This lab assignment focuses on the current-voltage characteristics of the *npn* bipolar-junction transistor, or NPN BJT. As you have discussed in lecture, when the transistor operates in the constant-current region the current through this device can be described by the simple equation

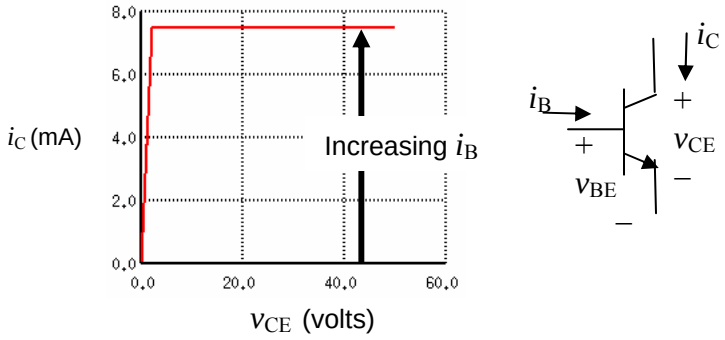
$$i_C = \beta i_B$$

Here i_C is the collector current, and i_B is the base current. The base current is determined by an equation that is very similar to that of the *pn*-junction diode:

$$i_B = I_S(e^{v_{BE}/\eta V_T} - 1)$$

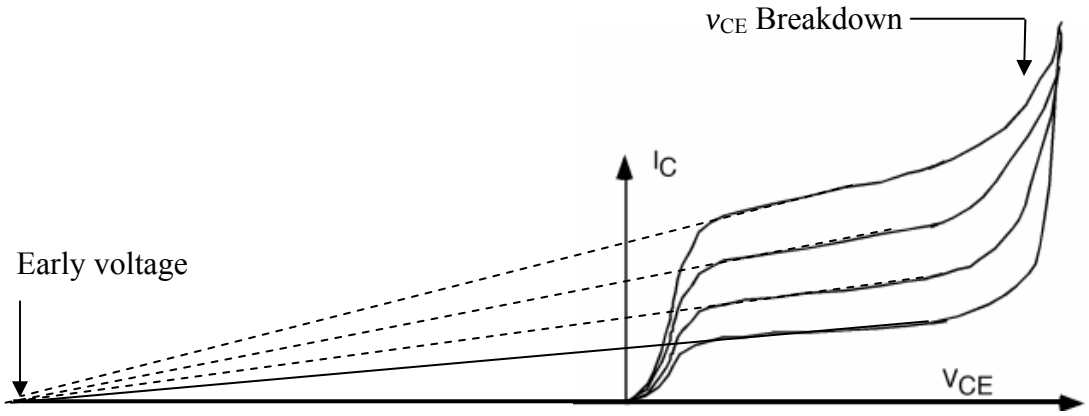
where the constant I_s is called the *scale* current, and $V_T = kT/q$ is the thermal voltage (about 25 mV at 25°C). In this lab, we'll again assume that $\eta = 1$ for our devices.

If we were to plot the characteristic of the BJT for a fixed value of i_B, it would look something like the following (the axis values are representative only):



Non-Ideal Behavior

In the idyllic world of EC410, we often assume that i_C and β in the constant-current region are constant for a given i_B, and that i_C does not change with v_{CE} . In the real world, this is not the case. Specifically, i_C changes with v_{CE}, causing the *i*-v curve to have non-zero slope in the "constant" current region. Also, the collector-emitter voltage cannot be increased arbitrarily, because the BJT's collector-emitter junction will breakdown at high values of v_{CE}. These non-ideal anomalies are depicted, for example, in the following *i*-*v* plot:



As you have may have learned in lecture, and as is discussed in the text, extending the transistor's constant-current curves into the left-hand quadrant causes them to intersect the voltage axis at the so-called *Early voltage*. This feature is shown in the above plot. (Note that the Early-voltage parameter is named after a person, not a time.). The breakdown value of v_{CE} is less definitive, because breakdown does not occur abruptly with increasing v_{CE} .

Laboratory Goal:	To plot the voltage-current characteristic of the 2N2222 bipolar transistor.
Learning Objectives:	BJT *v*-*i* characteristic, use of lab equipment, analysis techniques, simple BJT circuits, automated measurement techniques.
Suggested Tools:	Variable voltage source, multimeter, oscilloscope, op-amp circuits, diode logic circuits.

ASSIGNMENT

Level 1:

Devise a method for plotting the collector-emitter *i*-*v* curve of one your 2N2222 transistors. This plot should be displayed directly on the oscilloscope using the latter's *x*-*y* mode. For this purpose, you must do the following:

- Build a circuit capable of applying a varying voltage across the BJT's collector-emitter terminals while simultaneously applying that voltage to the *x*–axis of the oscilloscope.

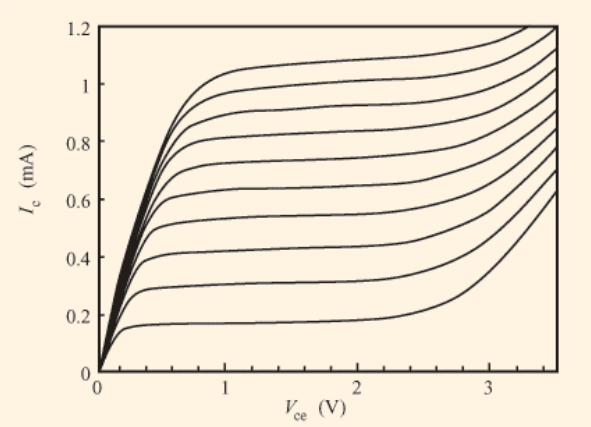
- Build a circuit capable of measuring the BJT's collector current i_C and converting the measured voltage to a proportional voltage. The latter must then be applied to the *y*-axis of the oscilloscope. In this way, the scope should display a graph of the collector current (*y*-axis) versus the collector emitter voltage (*x*-axis).

- Devise a method for adjusting the base current i_B so that you can observe the change in the i_C-v_{CE} plot as the value of i_B is changed. (Note: The behavior of the base-emitter junction is similar to that of a simple *pn*-junction diode. Specifically, if you apply a voltage greater than about 0.8 V directly across the base and emitter terminals, the base current will become so high that you are likely to burn out the BJT.

Level 2:
Use your instrumentation from Level 1 to measure the transistor's Early voltage and collector-emitter breakdown voltage. Make a table of the latter for several values of i_B.

Level 3: (Difficult)

The instrumentation that you developed in Level 1 is a useful tool for evaluating BJTs, MOSFETs, and any device that has a non-linear current-voltage characteristic. A far more useful tool, however, is one that displays many *i*-*v* curves at the same time, as in the following example:



Here, several representative values of i_B are chosen for the plot, with the understanding that the i_C-v_{CE} curve varies continuously between the curves that are chosen for plotting.

Goal: Revise the plotting system developed in Level 1 so that it displays several *i*-*v* curves a the same time. For this task, you will need to do the following:

- Develop a method for stepping i_B through a number of preset values.
- Synchronize the "sweep" of v_{CE} with the change of i_B so that a complete *i*-*v* curve is plotted between changes of i_B.

SOME HELPFUL TOOLS

Review the methods, discussed in EC410 Lab 1, for plotting the current-voltage characteristics of an electronic component.

For Level 3, you may want to utilize the properties of the 74HC163 Binary Counter included in your lab kit ("Presettable Synchronous 4-bit Binary Counter with Synchronous Reset"). You may also (possibly) need to use the usual collection of NAND and NOR gates included in your kit. The 74HC163 has the capability of counting in binary from **0000** to some preset maximum value less than or equal to **1111**. This chip may be useful in providing the needed base-current stepping an synchronization.
Here is an excerpt from the 74HC163 datasheet:

Presettable synchronous 4-bit binary counter; synchronous reset

74HC/HCT163

FEATURES

- Synchronous counting and loading
- Two count enable inputs for n-bit cascading
- Positive-edge triggered clock
- Synchronous reset
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT163 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT163 are synchronous presettable binary counters which feature an internal look-ahead carry and can be used for high-speed counting.
Synchronous operation is provided by having all flip-flops clocked simultaneously on the positive-going edge of the clock (CP).
The outputs (Q_0 to Q_3) of the counters may be preset to a HIGH or LOW level. A LOW level at the parallel enable input ($\overline{PE}$) disables the counting action and causes the data at the data inputs (D_0 to D_3) to be loaded into the counter on the positive-going edge of the clock (providing that the set-up and hold time requirements for $\overline{PE}$ are met). Preset takes place regardless of the levels at count enable inputs (CEP and CET).

For the "163" the clear function is synchronous.

A LOW level at the master reset input ($\overline{MR}$) sets all four outputs of the flip-flops (Q_0 to Q_3) to LOW level after the next positive-going transition on the clock (CP) input (provided that the set-up and hold time requirements for $\overline{MR}$ are met). This action occurs regardless of the levels at $\overline{PE}$, CET and CEP inputs.

This synchronous reset feature enables the designer to modify the maximum count with only one external NAND gate.

The look-ahead carry simplifies serial cascading of the counters. Both count enable inputs (CEP and CET) must be HIGH to count. The CET input is fed forward to enable the terminal count output (TC). The TC output thus enabled will produce a HIGH output pulse of a duration approximately equal to a HIGH level output of Q_0. This pulse can be used to enable the next cascaded stage.

The maximum clock frequency for the cascaded counters is determined by the CP to TC propagation delay and CEP to CP set-up time, according to the following formula:

$$f_{max} = \frac{1}{t_{P\,(max)}(\text{CP to TC}) + t_{SU}(\text{CEP to CP})}$$

You may also find it useful to build a simple, resistor-based digital-to-analog converter based on the op-amp summation amplifier. An example of such a circuit is shown below: