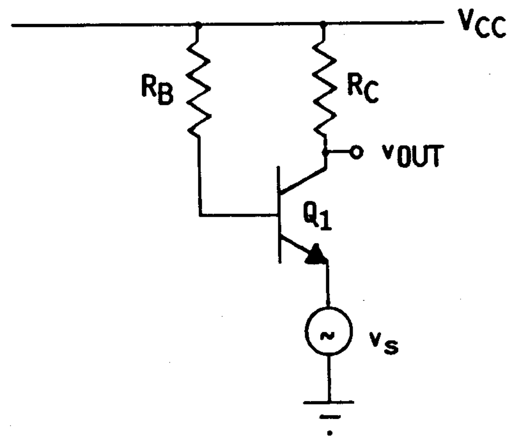
Chapter 8
Small-Signal Modeling of Three-Terminal Devices and Circuits

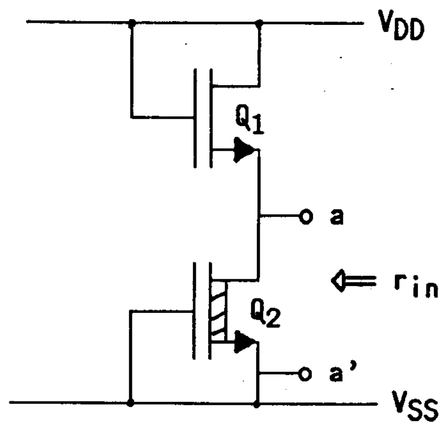
8.1 The BJT circuit shown below is excited by a signal source v_s.

a) Draw the incremental model of the circuit.

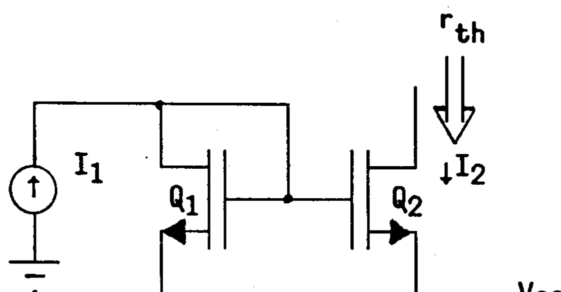
b) Find an expression for the small-signal gain v_{out}/v_s.



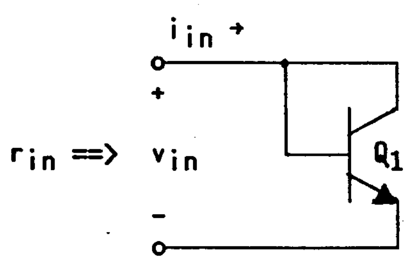
8.2 The MOSFETs shown below are biased in the constant-current region. Find an expression for the incremental resistance r_{in} that appears at the terminals a–a'



8.3 Consider the MOSFET current mirror shown below, in which I_1 is replicated as I_2. Find an expression for the small-signal input resistance r_{th} seen at the drain terminal of Q_2.



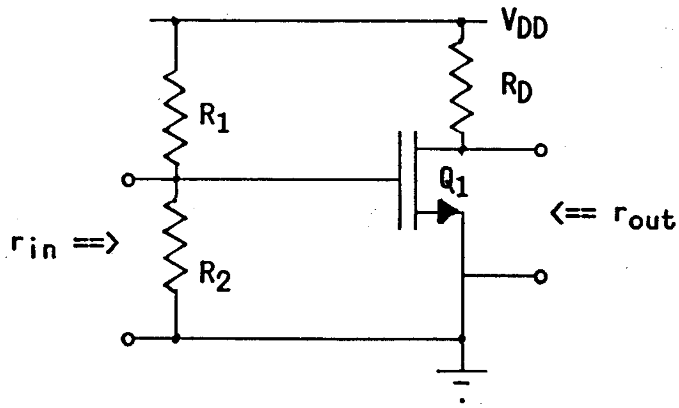
8.4 A BJT has its base connected to its collector, as shown below. If the device is biased in the constant-current region, find the incremental resistance r_{in} that appears between the collector and emitter terminals.



8.5 Consider the MOSFET amplifier shown below. Assume Q_1 to be biased in the constant-current region.

a) Find the incremental input resistance seen between the gate of Q_1 and ground.

b) Find the incremental output resistance seen between the drain of Q_1 and ground.

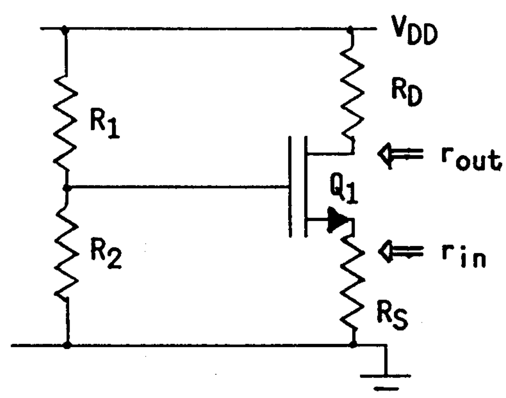


8.6 Repeat the previous problem if Q_1 is biased in the triode region.

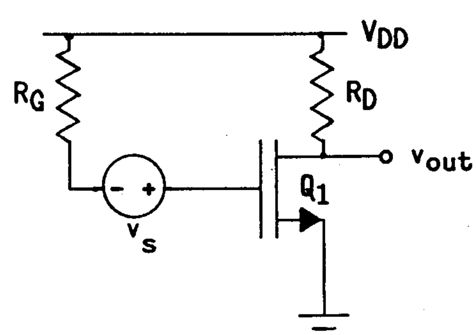
8.7 Consider the MOSFET amplifier shown below. Assume Q_1 to be biased in the constant-current region.

a) Find the incremental output resistance seen between the drain of Q_1 and ground.

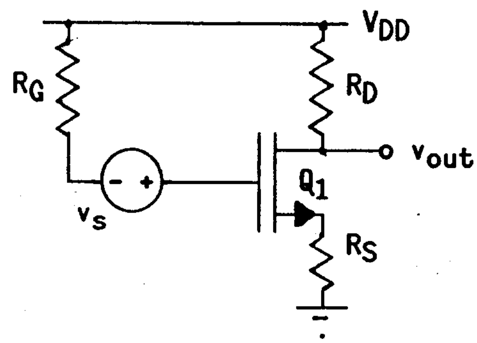
b) Find the incremental input resistance seen between the source of Q_1 and ground.



8.8 In the circuit shown below, the gate of Q_1 is driven by a small-signal voltage source v_s. Find the small-signal gain v_{out}/v_s if Q_1 is biased in the constant-current region



8.9 In the circuit shown below, the gate of Q_1 is driven by a small-signal voltage source v_s. Find the small-signal output v_{out} as a function of v_s if Q_1 is biased in the constant-current region. Note the resistor R_S connected between the source of Q_1 and ground.



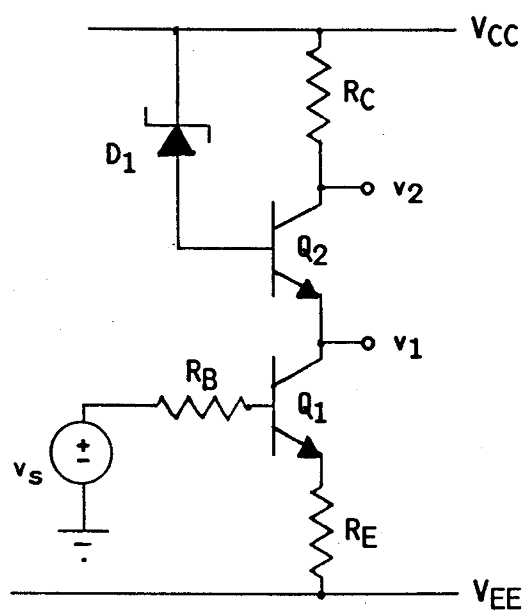
8.10 Repeat the previous problem if Q_1 is biased in the triode region.

8.11 Consider the BJT circuit shown below, in which Q_1 drives Q_2 in the tracking configuration.

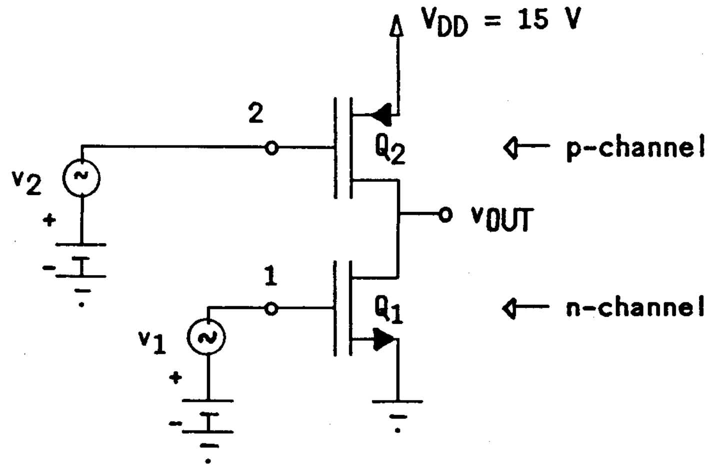
a) Find the small-signal gains v_1/v_s and v_2/v_s.

b) Find the small-signal output resistances seen at the v_1 and v_2 terminals (relative to ground).

c) Find the small-signal input resistance seen by v_s.



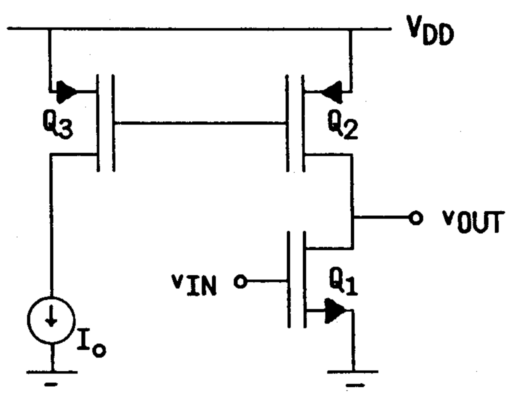
8.12 In the analog CMOS circuit shown below, assume Q_1 and Q_2 to be biased in the constant-current region.



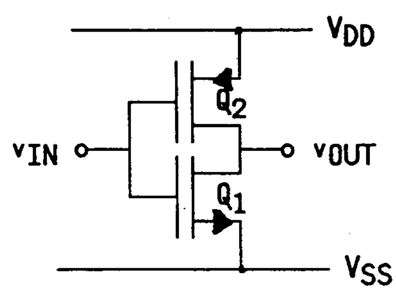
a) Find an expression for the small-signal gain v_{out}/v_1 if the signal component v_2 is zero.

b) Find an expression for the small-signal gain v_{out}/v_2 if the signal component v_1 is zero.

8.13 A CMOS inverter configuration is shown below. Q_1 is the inverting transistor and Q_2 functions as its active pullup load. Q_3 functions as a biasing current mirror. Find an expression for the small-signal gain v_{out}/v_{in}. Assume that v_{IN} contains an appropriate bias component so that Q_1 is biased in the constant current region.



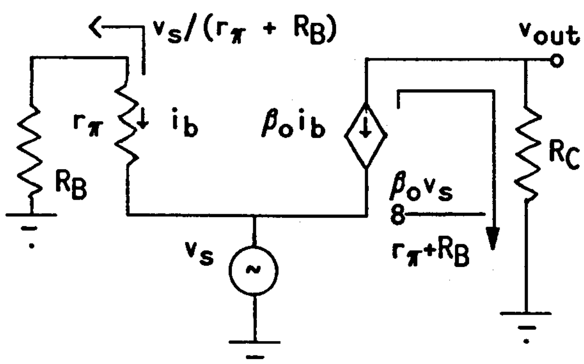
8.14 Find the small-signal output of the CMOS amplifier shown below. Assume that v_{IN} contains a dc bias component that biases both Q_1 and Q_2 into the constant current region.



Solutions

Chapter 8

8.1 Draw the incremental model of the circuit:

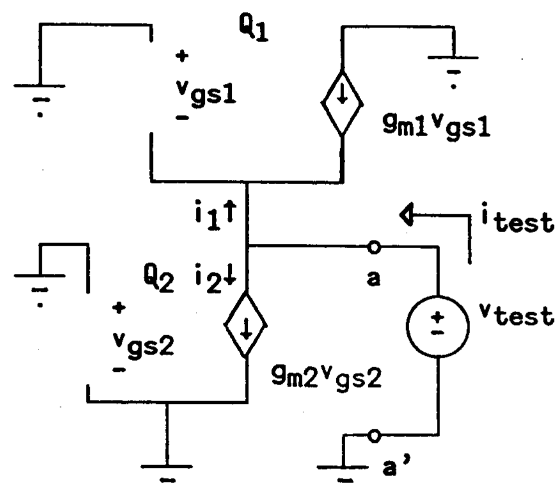


The voltage drop across r_π (defined as positive from the top of r_π to the bottom) is equal to $-v_s$. Hence $i_b = -v_s/(r_\pi + R_B)$. This current is replicated as $\beta_o i_b$ by the dependent source of the incremental model, so that a current $\beta_o v_s/(r_\pi + R_B)$ flows down into R_C in the direction shown.

This current causes the voltage v_{out} to be developed across R_C:

$$v_{out} = \beta_o \frac{R_C}{r_\pi + R_B} v_s$$

8.2 Here is an incremental model of the circuit with a test voltage applied to terminals a–a':

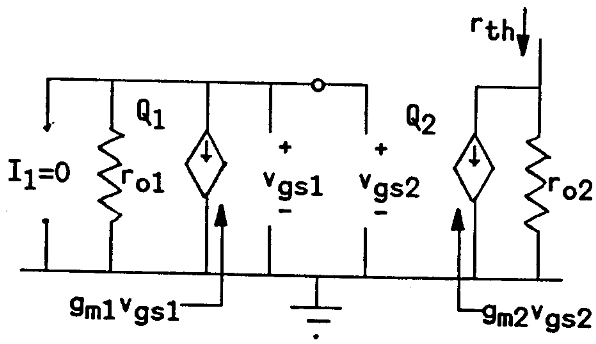


The v_{test} source fixes v_{gs1} to the value $-v_{test}$, so that $i_1 = -g_{m1}v_{gs1} = g_{m1}v_{test}$. Meanwhile, both sides of v_{gs2} are grounded, so that $v_{gs2} = 0$ and $i_2 = g_{m2}v_{gs2} = 0$. The current leaving the v_{test} source is thus equal to $i_{test} = i_1 + i_2 = g_{m1}v_{test}$.

The incremental input resistance at terminals a–a' is defined by

$$r_{in} = \frac{v_{test}}{i_{test}} = \frac{1}{g_{m1}}$$

8.3 The input resistance r_{th} can be found by examining the small-signal model of Q_2 and its surrounding circuit. The output resistance r_{o2} of Q_2 must be included in the model because no other external resistors are connected between the drain and source of Q_2; hence r_{o2} dominates. Note that the I_1 source becomes an open circuit in the incremental model:

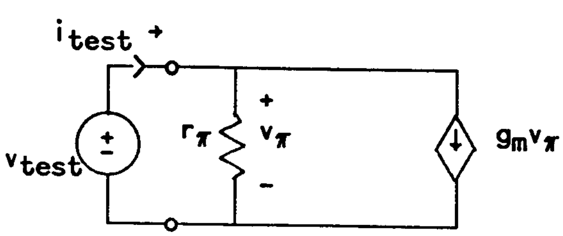


Taking KVL around the loop containing r_{o1} and v_{gs1} yields

$$g_{m1}v_{gs1}r_{o1} + v_{gs1} = 0$$

where the dependent source current $g_{m1}v_{gs1}$ flows up through r_{o1}. This KVL equation can be satisfied only if $v_{gs1} = 0$; v_{gs2} will also equal zero since $v_{gs2} = v_{gs1}$. The dependent source $g_{m2}v_{gs2}$, which is set to zero because v_{gs2}, becomes an open circuit, so that $r_{th} = r_{o2}$.

8.4 Here is the incremental model of the circuit that is valid when Q_1 is biased in the constant-current region. A "test" source has been connected to the r_{in} terminals:



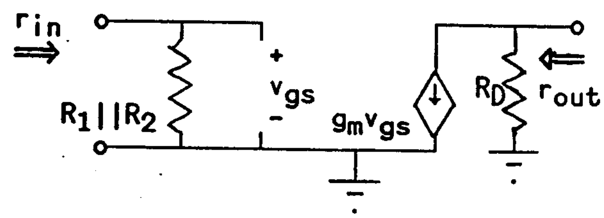
The test source sets v_π to the value v_{test}, so that i_{test} becomes

$$\frac{v_{test}}{r_\pi} + g_m v_{test}$$

The input resistance r_{in} is seen to be

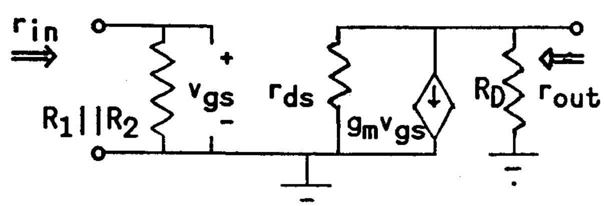
$$\frac{v_{test}}{i_{test}} = \left[\frac{1}{r_\pi} + g_m\right]^{-1} \equiv r_\pi \,\|\, \frac{1}{r_\pi}$$

8.5 Here is a small-signal model of the circuit that is valid when Q_1 is biased in the constant-current region



By inspection, $r_{in} = R_1||R_2$. For the circuit drawn as shown, $v_{gs} = 0$, so that the $g_m v_{gs}$ source becomes an open circuit and $r_{out} = R_D$. The output resistance r_{o1} of Q_1 has been omitted here since it would appear in parallel with R_D. The assumption is made that $r_{o1} >> R_D$.

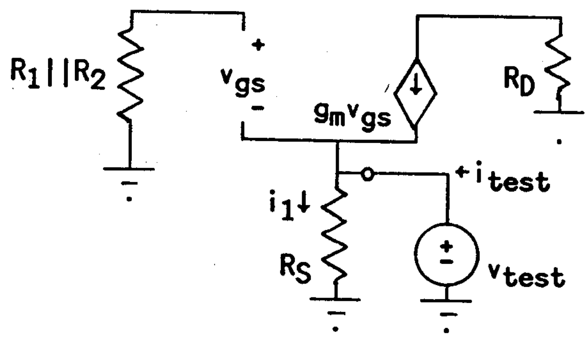
8.6 Here is a small-signal model of the circuit that is valid when Q_1 is biased in the triode region. The triode-region small-signal MOSFET model was derived in Section 8.3.



By inspection, $r_{in} = R_1||R_2$, as before. For the circuit drawn as shown, $v_{gs} = 0$, so that the $g_m v_{gs}$ source becomes an open circuit. The output resistance thus becomes $r_{out} = R_D||r_{ds}$, where

$$r_{ds} = [2K(V_{GS} - V_{TR})]^{-1}$$

8.7 Construct a small-signal model of the circuit using the constant-current region model for Q_1. The input resistance can be found by applying a test source to R_S:



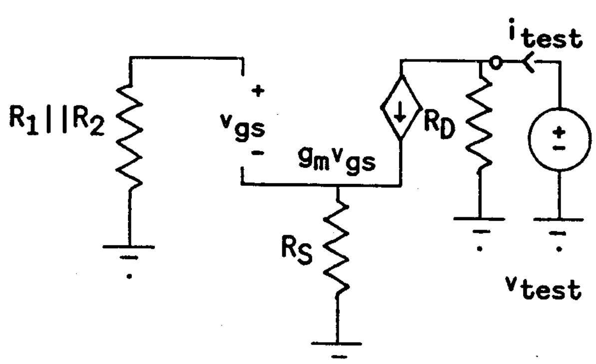
The applied source fixes v_{gs} to the value $-v_{test}$, so that i_{test}, which has two components, becomes

$$i_1 - g_m v_{gs} = \frac{v_{test}}{R_S} + g_m v_{test}$$

The incremental resistance r_{in} is equal to v_{test}/i_{test}, i.e.,

$$r_{in} = \left[\frac{1}{R_S} + g_m\right]^{-1} \equiv R_S \left|\right| \frac{1}{g_m}$$

The incremental output resistance r_{out} can be found in a similar manner by applying a test source between the drain of Q_1 and ground:



In this case, KVL taken around the loop containing v_{gs} yields

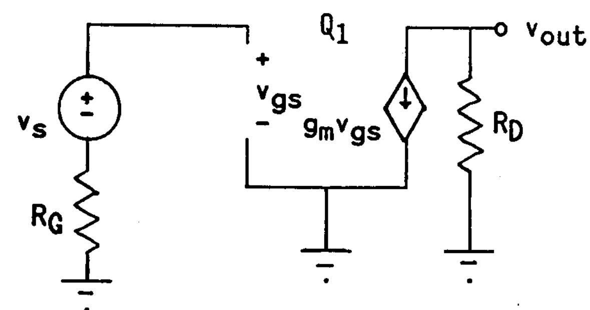
$$v_{gs} + g_m v_{gs} R_S = 0$$

where the current $g_m v_{gs}$ flows through R_S and the current through $R_1||R_2$ is zero. This KVL equation can only be satisfied for the condition $v_{gs} = 0$. With $v_{gs} = 0$, the dependent source becomes an open circuit, so that

$$r_{out} = \frac{v_{test}}{i_{test}} = R_D$$

The output resistance r_o of Q_1, assumed to be much larger than R_D, has been omitted from the model.

8.8 The gain of the amplifier can be found by constructing its small-signal model:

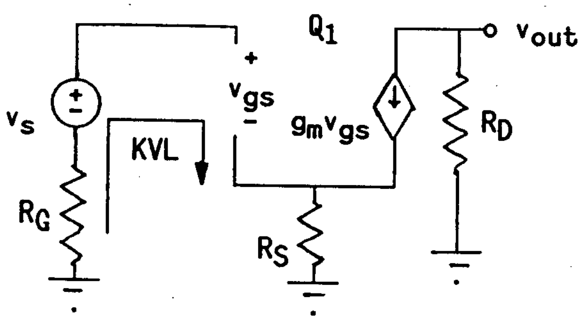


In this incremental circuit, the voltage v_{gs} is equal to v_s. Note that no current flows through R_G, hence the voltage drop across R_G is zero. The dependent current source pulls a current $g_m v_{gs}$ up from ground through R_D, so that the small-signal output becomes

$$v_{out} = -g_m v_{gs} R_D = -g_m R_D v_s$$

The small-signal gain of this amplifier, defined by v_{out}/v_s, is $-g_m R_D$.

8.9 Here is the small-signal model of the amplifier, formed by setting V_{DD} to zero:



From KVL around the input loop:

$$v_s = v_{gs} + g_m v_{gs} R_S$$

Note that the voltage drop across R_G is zero because the current through it is zero. Solving the KVL equation for v_{gs} results in

$$v_{gs} = \frac{v_s}{1 + g_m R_S}$$

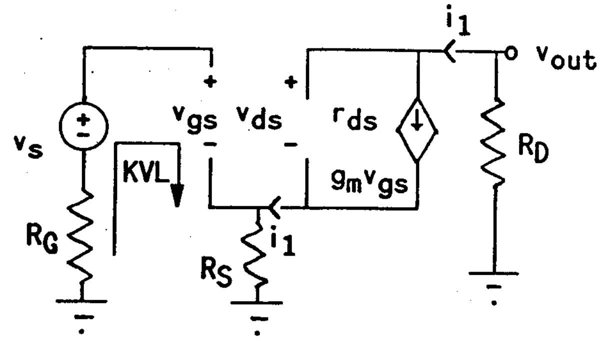
The dependent source pulls a current $g_m v_{gs}$ up from ground through R_D, so that the output becomes

$$v_{out} = -g_m v_{gs} R_D = v_s \frac{-g_m R_D}{1 + g_m R_S}$$

The small signal gain of this amplifier, defined by v_{out}/v_s, is

$$\frac{-g_m R_D}{1 + g_m R_S}$$

8.10 Here is an incremental model of the circuit that is valid when Q_1 is biased in the triode region (see Sec. 8.3 for the derivation of the triode region small-signal MOSFET model):



As derived in Sec. 8.3,

$$r_{ds} = [2K(V_{GS} - V_{TR})]^{-1}$$

and $\quad g_m = 2KV_{DS}$.

The current i_1 is equal to the sum of the dependent source current $g_m v_{gs}$ plus the current that flows downward through r_{ds}, i.e.

$$i_1 = g_m v_{gs} + v_{ds}/r_{ds}$$

Note that i_1 is the current pulled up from ground through R_D and is also the current flowing down into R_S. The drain-to-source voltage v_{ds} is given by

$$v_{ds} = v_{out} - i_1 R_S = -i_1 R_D - i_1 R_S$$

Using this expression for v_{ds}, the previous equation for i_1 becomes

$$i_1 = g_m v_{gs} - i_1 \frac{R_D + R_S}{r_{ds}}$$

KVL taken around the input loop of the circuit results in

$$v_{gs} = v_s - i_1 R_S$$

Substituting this equation for v_{gs} into the expression for i_1 results in

$$i_1 = g_m(v_s - i_1 R_S) - i_1 \frac{R_D + R_S}{r_{ds}}$$

Solving for i_1 results in

$$i_1 = \frac{g_m v_s}{1 + g_m R_S + (R_D + R_S)/r_{ds}}$$

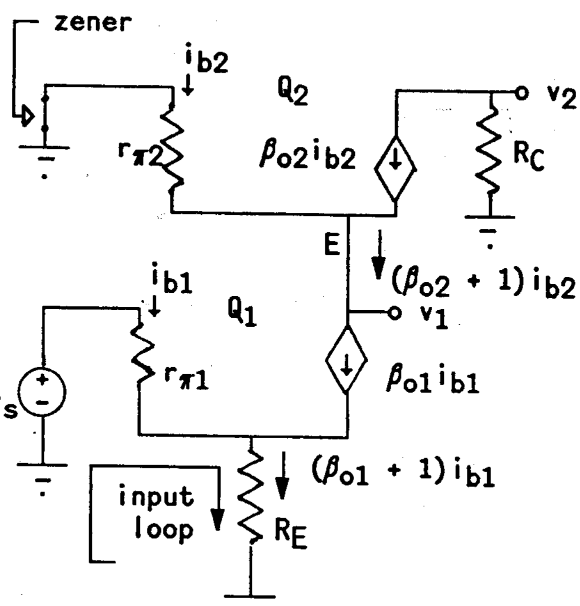
The output of the circuit is given by

$$v_{out} = -i_1 R_D$$

$$= \frac{-g_m R_D}{1 + g_m R_S + (R_D + R_S)/r_{ds}} v_s$$

8.11 The purpose of D_1 is to provide a bias voltage of value $V_{CC} - V_{ZK}$ at the base of Q_2. To the extent that the incremental resistance r_z of the zener can be neglected, the zener will behave as a dc voltage source and will not affect the small-signal behavior of the circuit.

Here is an incremental representation of the amplifier:



a) Find the small-signal gains measured at v_1 and v_2. From KVL around the input loop,

$$v_s = i_{b1} r_{\pi 1} + (\beta_{o1} + 1) i_{b1} R_E,$$

or

$$i_{b1} = \frac{v_s}{r_{\pi 1} + (\beta_{o1} + 1) R_E}$$

The current $\beta_{o1} i_{b1}$ from the collector of Q_1 is pulled down through the emitter of Q_2 so that, via KCL at node E, $\beta_{o1} i_{b1} = (\beta_{o2} + 1) i_{b2}$, or

$$i_{b2} = \frac{\beta_{o1}}{\beta_{o2} + 1} i_{b1}$$

$$= \frac{\beta_{o1}}{\beta_{o2} + 1} \frac{v_s}{[r_{\pi 1} + (\beta_{o1} + 1) R_E]}$$

The output v_1 is equal to $-i_{b2} r_{\pi 2}$. Substitution of the above expression for i_{b2} yields

$$v_1 = \frac{-\beta_{o1}}{\beta_{o2} + 1} \frac{r_{\pi 2}}{[r_{\pi 1} + (\beta_{o1} + 1) R_E]} v_s$$

The output v_2 is equal to $-\beta_{o2} i_{b2} R_C$, which becomes

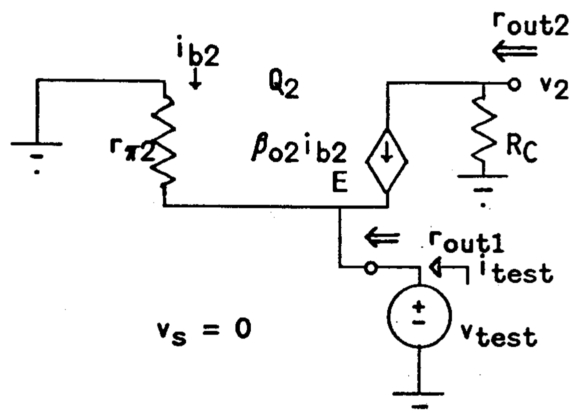
$$v_2 = \frac{-\beta_{o2} \beta_{o1}}{\beta_{o2} + 1} \frac{R_C}{[r_{\pi 1} + (\beta_{o1} + 1) R_E]} v_s$$

In the limit of large β_{o1} and β_{o2}, v_1 and v_2 become

$$v_1 \simeq \frac{-r_{\pi 2}}{\beta_{o1} R_E} v_s \quad \text{and} \quad v_2 = \frac{-R_C}{R_E} v_s$$

If Q_1 and Q_2 are matched (same β_o), v_1 becomes $-v_s / g_m R_E$

b) Use the test source method to find r_{out1} and r_{out2}. When v_s is set to zero, both i_{b1} and the $\beta_{o1} i_{b1}$ dependent source are also set to zero in the incremental model. The output resistance at v_1 can be found by applying a test source between the v_1 terminal and ground:



From the test circuit shown above, i_{b2} becomes $-v_{test}/r_{\pi 2}$, so that i_{test} becomes

$$-(\beta_{o2} + 1) i_{b2} = (\beta_{o2} + 1) \frac{v_{test}}{r_{\pi 2}}$$

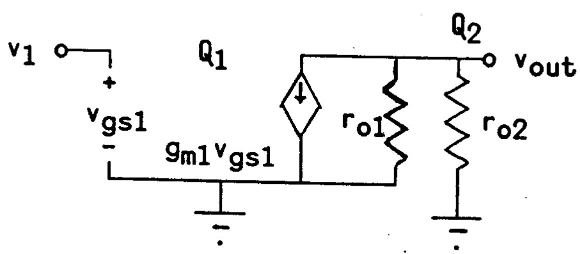
The incremental resistance r_{out1}, defined by v_{test}/i_{test}, becomes $r_{\pi 2}/(\beta_{o2} + 1)$.

By a similar procedure, the output resistance r_{out2} at the v_2 terminal is seen to be R_C.

c) The input resistance r_{in} seen by v_s will be equal to v_s/i_{b1}. From the previously derived expression for i_{b1},

$$r_{in} = \frac{v_s}{v_s/[r_{\pi 1} + (\beta_{o1}+1)R_E]}$$
$$= r_{\pi 1} + (\beta_{o1} + 1)R_E.$$

8.12 a) Here is an incremental model of the circuit when the signal component v_2 is equal to zero:



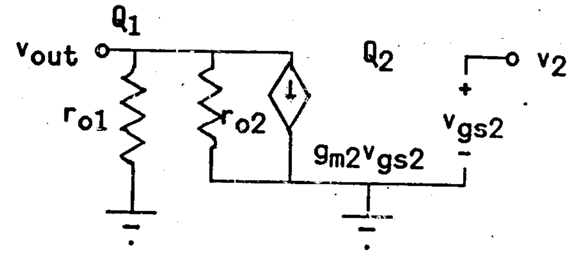
Note that r_{o1} and r_{o2} must be included in the model, because no smaller resistances appear in parallel. This feature is characteristic of many CMOS circuits.

With the signal component v_2 equal to zero, the incremental model of the pullup device Q_2 reduces to just r_{o2}. With $v_{gs1} = v_1$, the small-signal output of this circuit becomes

$$v_{out} = -g_{m1}(r_{o1} || r_{o2})v_1$$

i.e., a gain equal to $-g_{m1}(r_{o1}||r_{o2})$.

b) Here is an incremental model of the circuit when the signal component v_1 is equal to zero:



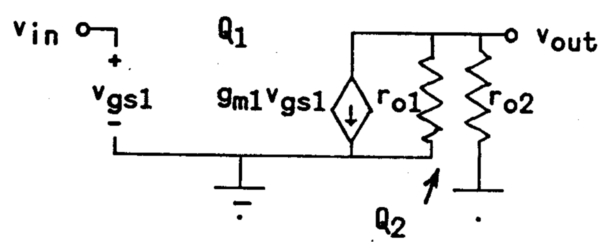
From this circuit,

$$v_{out} = -g_{m2}(r_{o1}||r_{o2})v_2$$

The output from both input signals, found by superposition, becomes

$$v_{out} = -(g_{m1}v_1 + g_{m2}v_2)(r_{o1}||r_{o2})$$

8.13 The small-signal model of the circuit is shown below. The incremental output resistance of Q_2 functions as the load to Q_1. The output resistance of Q_1 must also be included in the model because no smaller external resistor appears in parallel.



By inspection, $v_{gs1} = v_{in}$. The dependent source pulls current up through the parallel combination $r_{o1}||r_{o2}$, so that the output becomes

$$v_{out} = -g_{m1}(r_{o1}||r_{o2})\, v_{in}$$
$$= -2\sqrt{K_1 I_{D1}}(r_{o1}||r_{o2})\, v_{in}$$

Note that Q_1 and Q_2 share the same I_D; $r_{o1}||r_{o2}$ can thus be expressed as

$$\frac{\frac{V_{A1}}{I_D} \cdot \frac{V_{A2}}{I_D}}{V_{A1}/I_D + V_{A2}/I_D} = \frac{V_{A1} \cdot V_{A2}}{(V_{A1} + V_{A2})I_D}$$

where V_{A1} and V_{A2} are the Early voltages of Q_1 and Q_2, respectively.