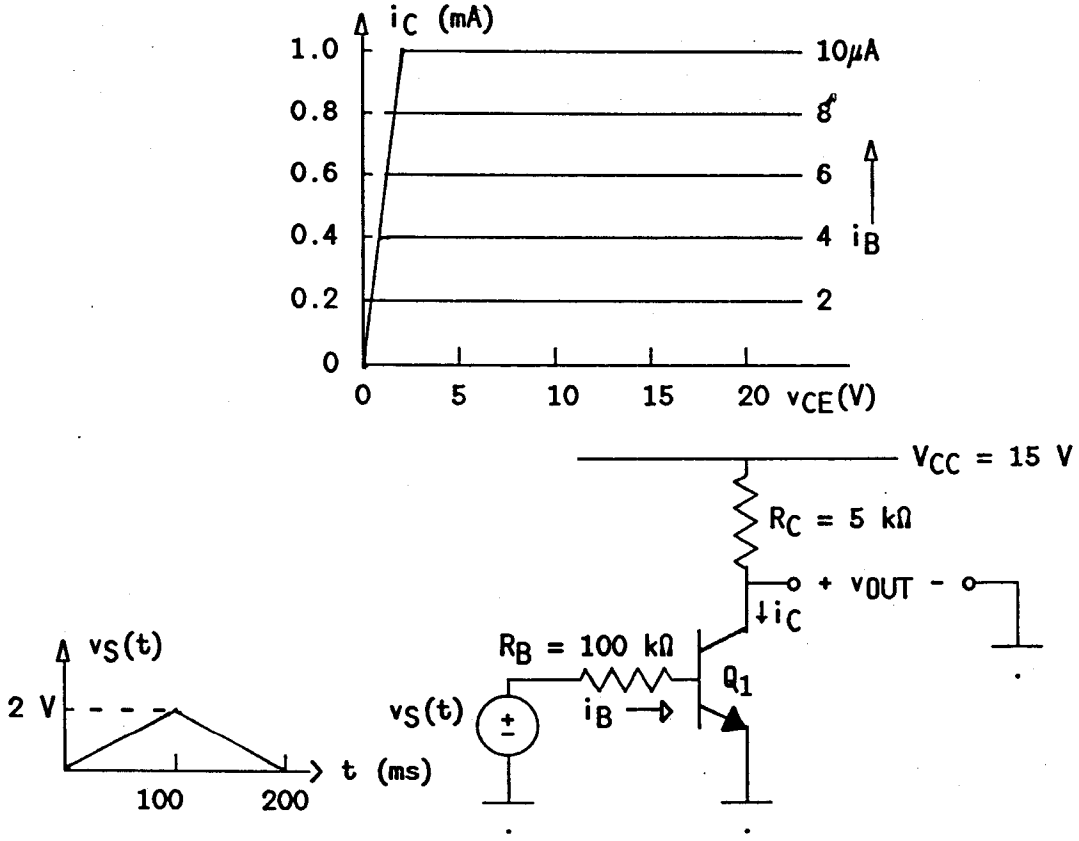
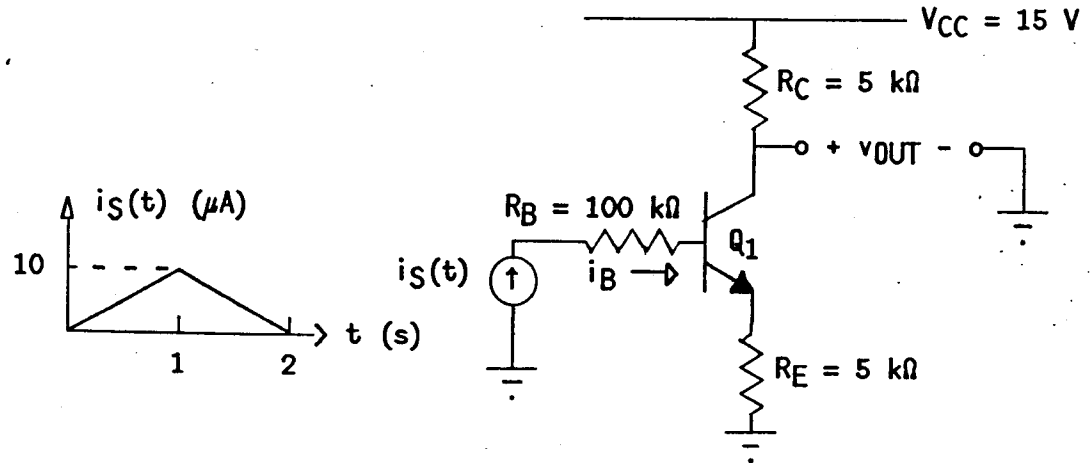
6.1 A bipolar junction transistor (BJT) has the v-i characteristics shown below. The device is connected to a simple inverter circuit whose input consists of a triangular voltage pulse $v_S(t)$ that rises from zero to 2 V in 100 ms, then falls to zero after another 100 ms. Find the resulting output voltage $v_{OUT}(t)$. Assume that $V_f = 0.7$ V for the base-emitter junction of Q_1.



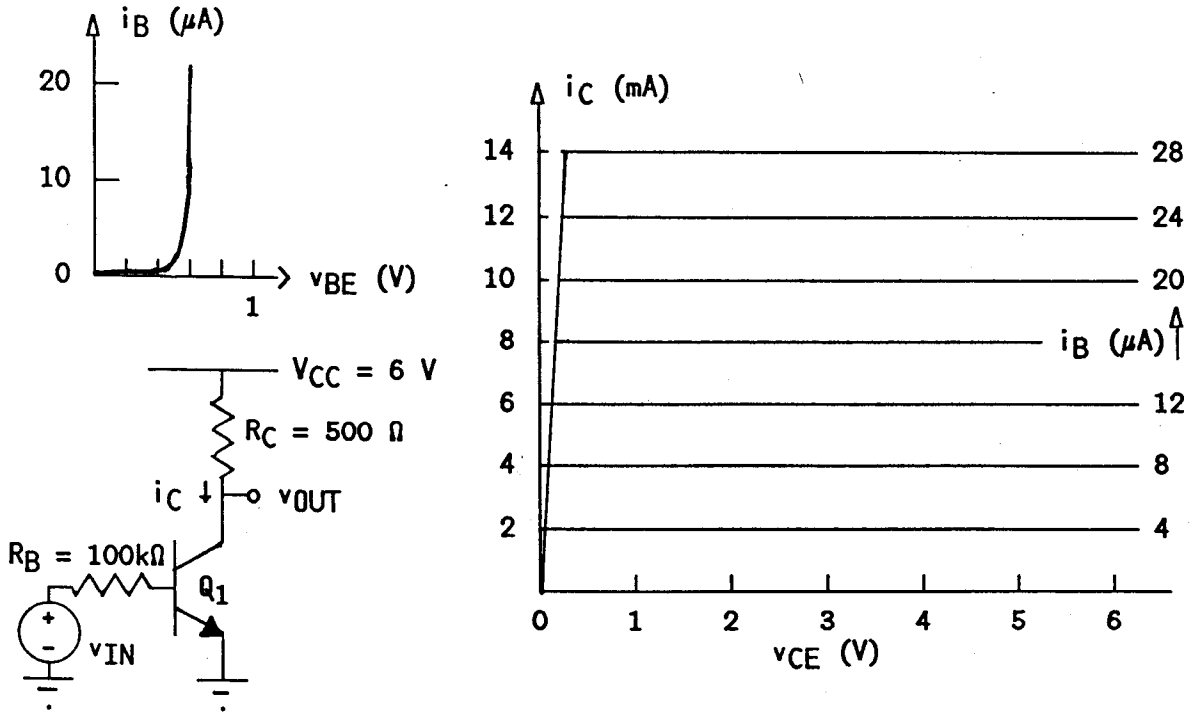
6.2 Repeat Prob 6.1 if R_C is changed from 5 kΩ to 25 kΩ.

6.3 A bipolar junction transistor (BJT) has the v-i characteristics shown in Prob. 6.1. The device is connected to the circuit shown below. The input consists of a triangular current pulse $i_S(t)$ that rises from zero to 10 μA in 1 s, then falls to zero after another 1 s. Find the output voltage $v_{OUT}(t)$. Assume that $V_{BE} = V_f = 0.7$ V when $i_B > 0$.



6.4 Repeat Prob 6.3 if R_C and R_E are both changed from 5 kΩ to 50 kΩ.

6.5 An NPN BJT with the v-i characteristics shown below is connected in a basic inverter circuit with resistive pullup load. Use the graphical technique to plot the voltage transfer characteristic of the inverter over the input range -2 V < v_{IN} < 5 V.



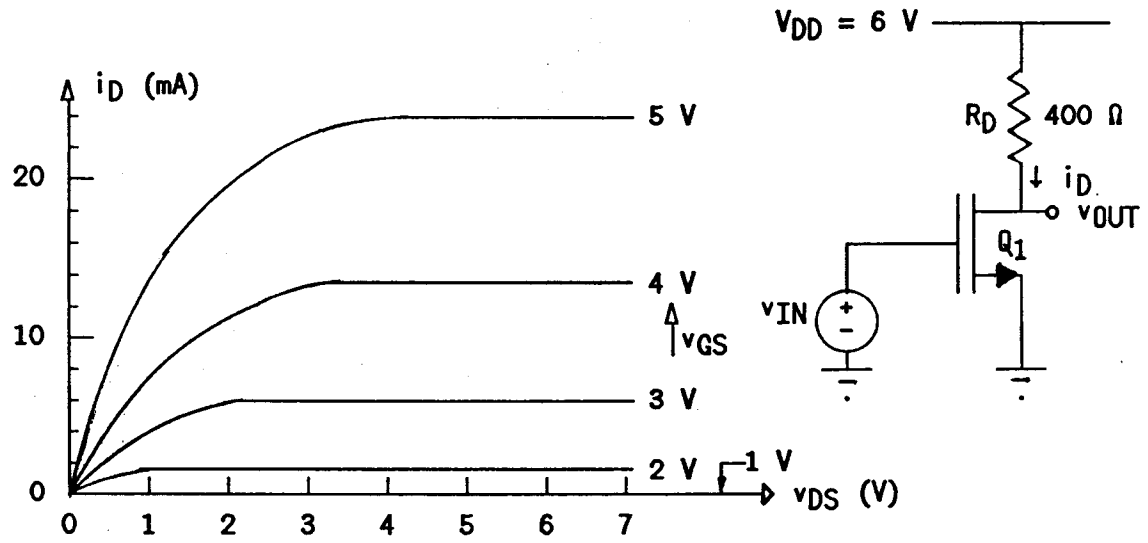
6.6 Consider the BJT inverter circuit of Prob. 6.5. The BJT has the v-i characteristics shown above.

a) What is the value of β_F for this BJT?

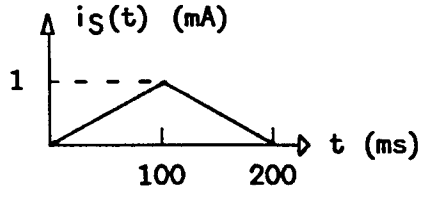
b) For v_{IN} = 2.5 V, find i_C and v_{OUT} using analytical methods.

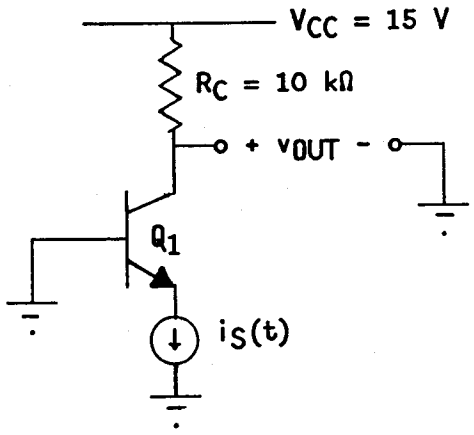
c) The BJT is now replaced by a device with twice the value of β_F. What happens to the values of i_C and v_{OUT} computed in part b)?

6.11 An enhancement-mode n-channel MOSFET having the v-i characteristics shown below is connected in a basic inverter circuit with resistive pullup load, as indicated. Use the graphical technique to plot the voltage transfer characteristic of the inverter.



6.12 A bipolar junction transistor (BJT) has the v-i characteristics given in Prob. 6.1. The device is connected to the circuit shown below. The input consists of a triangular current pulse $i_S(t)$ that rises from zero to 1 mA in 100 ms, then falls to zero after another 100 ms. This current is drawn from the emitter terminal of Q_1, which is connected in the tracking configuration. Find the output voltage $v_{OUT}(t)$.



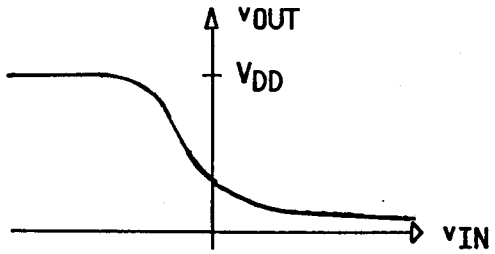


6.13 Repeat Prob. 6.12 if R_C is changed from 10 kΩ to 20 kΩ.

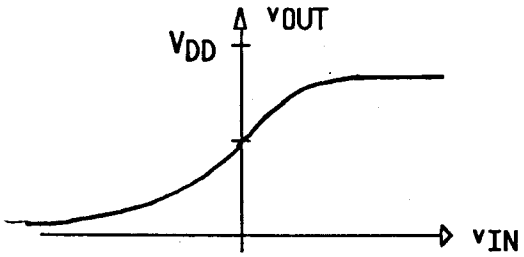
6.14 Design a new version of the tracking circuit of Prob. 6.12 that has as its input a voltage source $v_S(t)$. The v_S input source should directly produce an equivalent tracked input current i_S.

6.7 Consider the BJT inverter circuit of Prob. 6.5. The BJT has the v-i characteristics shown. Use analytical methods to find the slope dv_{OUT}/dv_{IN} when the BJT operates in its active (constant-current) region.

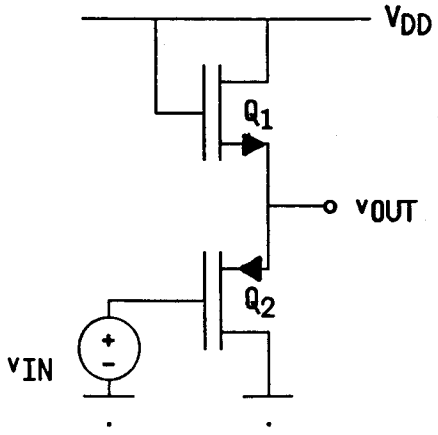
6.8 Using identical n-channel MOSFETs only, design a circuit for which the voltage transfer characteristic has the basic form shown below.



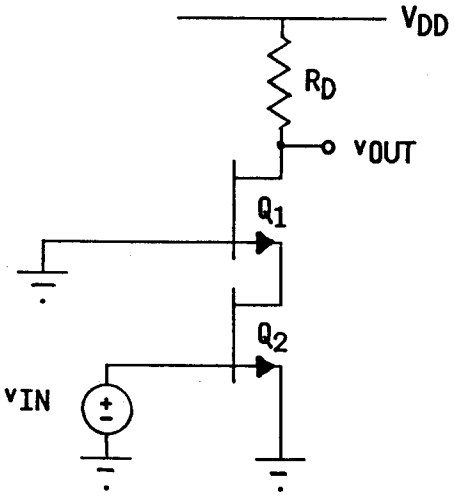
6.9 Using only n-channel and p-channel depletion-mode MOSFETs, design a CMOS circuit whose voltage transfer characteristic has the basic form shown below. Note that v_{OUT} is equal to $V_{DD}/2$ at $v_{IN} = 0$. The circuit drives a load resistance R_L.



6.10 Determine the general form of the voltage transfer characteristic of the NMOS/PMOS (CMOS) circuit shown below



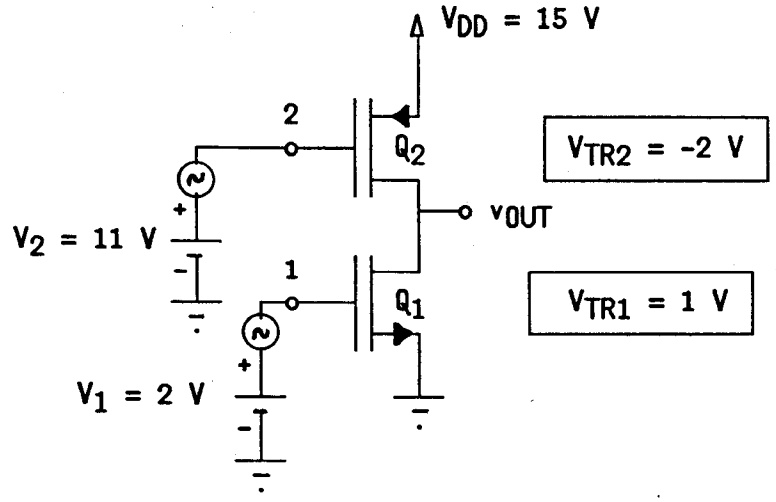
6.15 Find the transfer characteristic of the JFET circuit shown below. The devices have the same values of V_P and I_{DSS}.



6.16 In the CMOS circuit shown below, nodes 1 and 2 are connected to signal sources that contain dc components of 2 V and 11 V, respectively.

a) For what range of v_{OUT} is Q_1 in the constant-current region?

b) For what range of v_{OUT} is Q_2 in the constant-current region?



6.17 Consider the CMOS circuit described in Prob 6.16. Suppose that the two inputs are connected together and driven by a common input source v_{IN}. Make a qualitative sketch of the resulting v_{IN}-v_{OUT} transfer characteristic.

Chapter 6

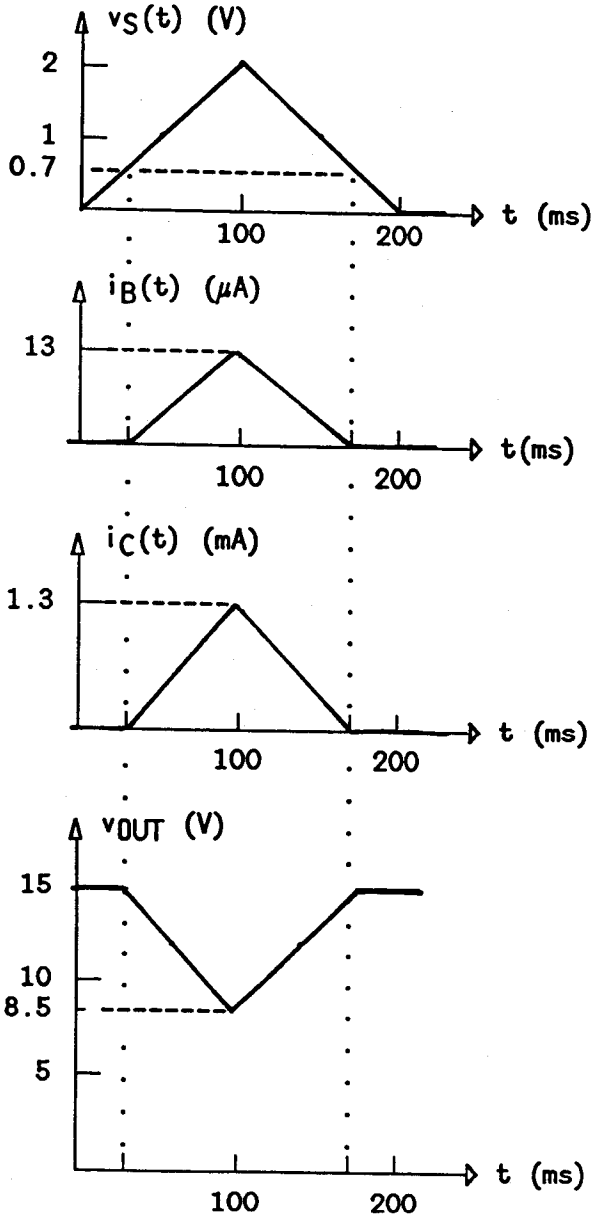
Solutions

6.1 Application of KVL to the output loop of this circuit yields $v_{OUT} = V_{CC} - i_C R_C$. The next step involves determining i_C as a function of v_S. For input voltages $v_S < V_f$, the base-emitter junction of Q_1 will not be forward biased, and the transistor will be in cutoff. Under cutoff conditions, both i_B and i_C will be zero and v_{OUT} will equal V_{CC}.

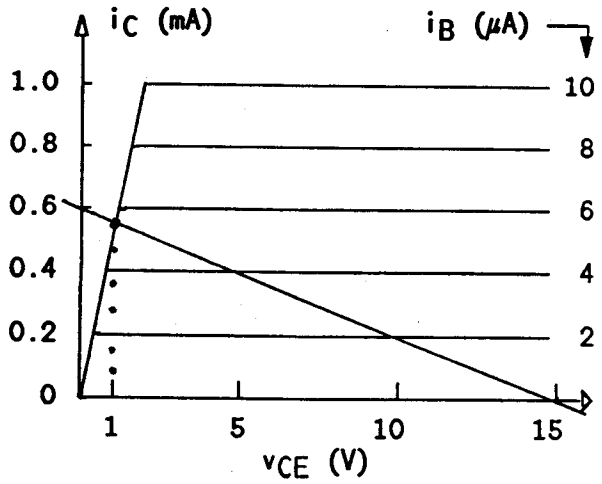
For values of v_S larger than V_f, application of KVL to the input loop of the circuit yields $i_B = (v_S - V_f)/R_B$. At the peak value of v_S, i_B will be equal to $(2\ V - 0.7\ V)/(100\ k\Omega) = 13\ \mu A$. When v_S again falls below 0.7 V, i_B will fall back to zero.

For $v_S > V_f$, i_B will rise and fall linearly with v_S. An inspection of the BJT v-i characteristics reveals that $i_C/i_B = \beta_F = 100$ in the BJT's constant-current region. As long as the BJT does not reach saturation, i_C will thus increase linearly with v_S for $v_S > V_f$ and will be equal to $i_C = \beta_F(v_S - V_f)/R_B$. At the peak value of

v_S, i_C will be equal to 100(13 μA) = 1.3 mA. For this value of i_C, v_{OUT} becomes $V_{CC} - i_C R_C$ = 15 V - (1.3 mA)(5 kΩ) = 8.5 V. This value of v_{OUT}, which is also the value of v_{CE} for the BJT, is well in excess of V_{sat}, indicating that the BJT does not reach saturation, even at the peak value of v_S. Plots of $v_S(t)$, $i_B(t)$, $i_C(t)$, and $v_{OUT}(t)$ are shown below.



6.2 The base-emitter loop of the modified circuit is identical to that of the original, so that i_B again reaches a peak of 13 μA when v_S = 2 V. In this case, however, the larger value of R_C causes a larger proportional drop in v_{OUT} for the same change in i_C. The BJT reaches its saturation point $v_{CE} = V_{sat}$ before the peak of v_S is reached. The exact values of i_C and v_{CE} at saturation can be found by plotting the load line of V_{CC} and R_C over the v-i characteristics of the BJT:



With R_C = 25 kΩ, the intercepts of the load line are V_{CC} = 15 V (open circuit voltage of the Thevenin circuit formed by V_{CC} and R_C) and V_{CC}/R_C = 0.6 mA (short circuit current of the Thevenin circuit).

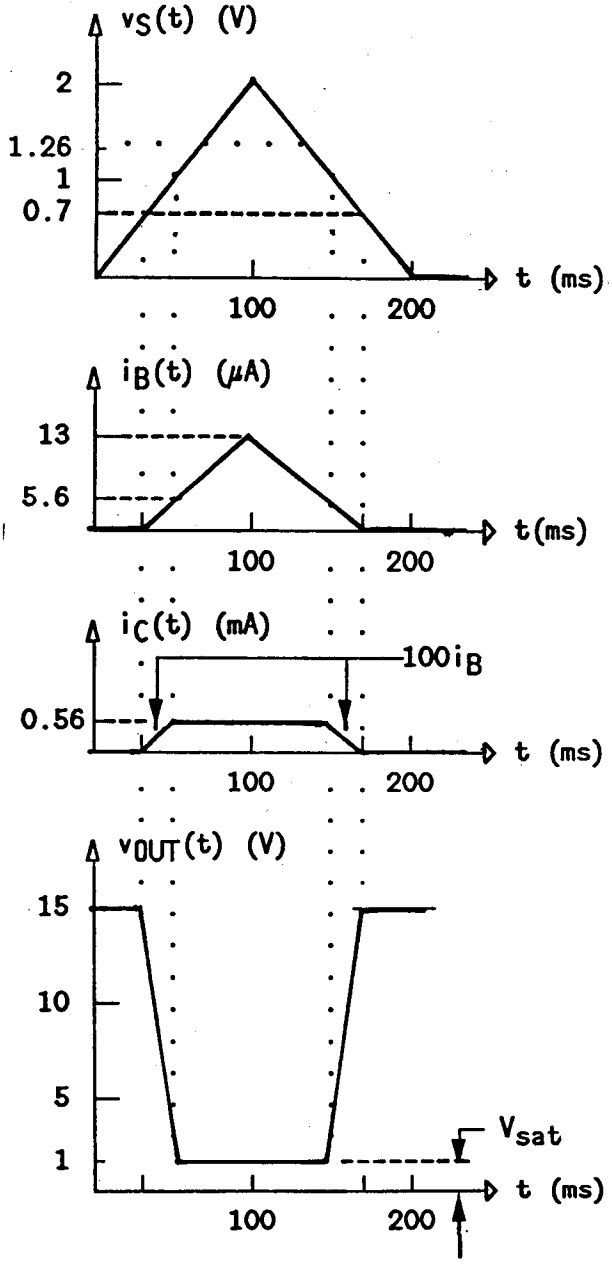
As is evident from the figure, the BJT reaches saturation when $v_{CE} \simeq 1$ V and i_C = 0.56 mA. This latter value can be confirmed by applying KVL to the output loop of the circuit with $v_{CE} = V_{sat}$, yielding

$$i_C = \frac{V_{CC} - V_{sat}}{R_C} = \frac{15\text{V} - 1\text{V}}{25\ \text{k}\Omega} = 0.56\ \text{mA}$$

The i_B value corresponding to arrival at this saturation point is given by

(0.56 mA)/100 = 5.6 μA, for which v_{IN} = 1.26 V.

For a given v_S, the value of i_B will be the same as that found in Prob 6.1. For the modified circuit, i_C will rise with i_B as $\beta_F i_B$ until the BJT saturates. For larger values of v_S, i_B will increase but i_C will remain constant. Similarly, v_{OUT} will fall linearly with rising v_S and i_B until it reaches the value V_{sat} and will remain constant thereafter. Plots of $v_S(t)$, $i_B(t)$, $i_C(t)$, and the resulting $v_{OUT}(t)$ are shown to the right. ====>



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6.3 The value of V_f for the base-emitter junction of the BJT is irrelevant to this problem. The current source $i_S(t)$ forces its current into the base of Q_1 regardless of the value of v_{BE}. The voltage across the i_S source adjusts itself to be whatever value of v_{BE} is required for the established i_B.

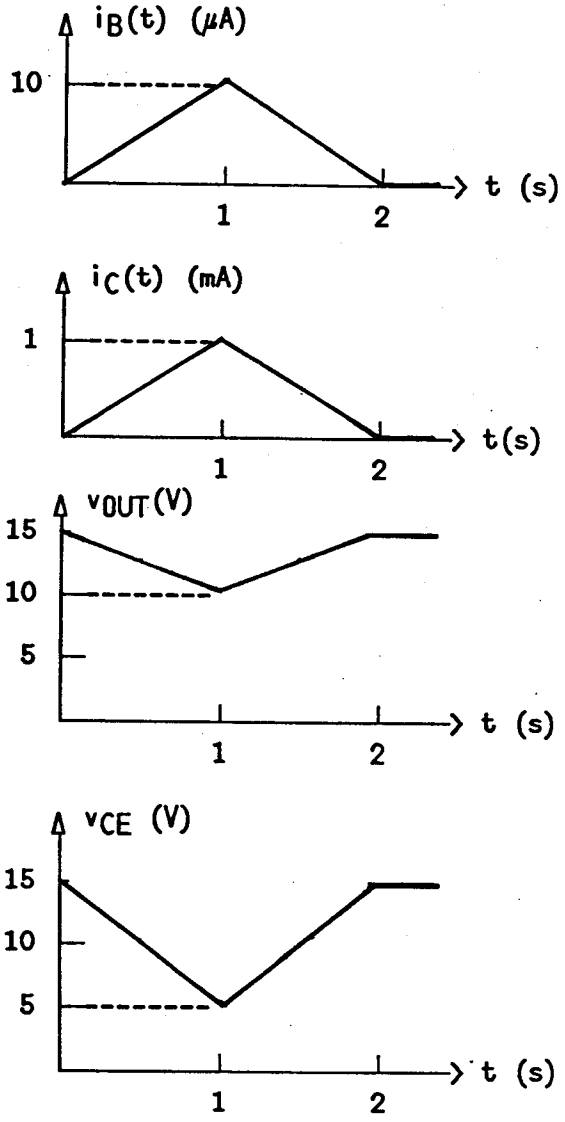
For a given instantaneous value of i_S, the value of i_C will be equal to $\beta_F i_B$ provided that Q_1 does not saturate. The resulting output voltage becomes $v_{OUT} = V_{CC} - i_C R_C$, where $v_{CE} = V_{CC} - i_C R_C - i_E R_E$. Since $\beta_F \gg 1$ it follows that $i_E \simeq i_C$, so that

$$v_{CE} \simeq V_{CC} - i_C(R_C + R_E)$$

Knowledge of v_{CE} is needed to determine when Q_1 goes into saturation.

At the peak value of i_S, i_C will equal $\beta_F i_S = 100(10\ \mu A) = 1$ mA, so that $v_{OUT} = 15$ V $-$ (1 mA)(5 kΩ) = 10 V. Note that $v_{CE} = 15$ V $-$ (1 mA)$\times$ (5 kΩ + 5 kΩ) = 5 V at the peak of i_S. This v_{CE} voltage is clearly above V_{sat}, indicating that the BJT is never driven into saturation.

Plots of $i_B = i_S$, i_C, v_{OUT}, and v_{CE} versus time are shown to the right. Note that i_C, v_{OUT}, and v_{CE} all change linearly with i_S.



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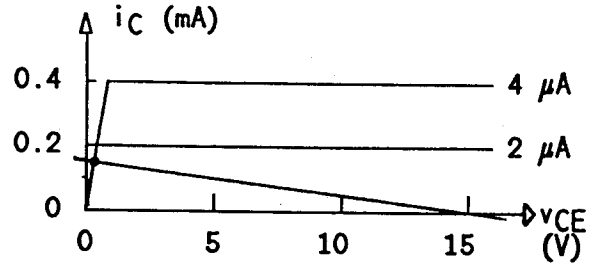
6.4 As in the circuit of Prob 6.3, i_B will again be equal to i_S. In this case, however, the larger values of R_C and R_E will cause a larger proportional drop in v_{OUT} and v_{CE} for the same increase in i_C. Thus Q_1 will reach its saturation point, with $v_{CE} = V_{sat}$, before the peak of i_S is reached. The exact values of i_C and v_{CE} at saturation can be found by plotting the load line of the voltage V_{CC} and total resistance $(R_C + R_E)$ over the BJT v-i characteristics:



With $R_C = R_E = 50$ kΩ, the intercepts of the load line are $V_{CC} = 15$ V (open circuit voltage of the Thevenin circuit formed by V_{CC}, R_C, and R_E) and $V_{CC}/(R_C + R_E) = 0.15$ mA (short circuit current of the Thevenin circuit). As is evident from the figure, the BJT reaches saturation when $v_{CE} \simeq 0.2$ V and $i_C \simeq 0.15$ mA. This latter value can be confirmed by applying KVL to the output loop of the circuit with $v_{CE} = V_{sat}$, yielding

$$i_{C\text{-}sat} = \frac{V_{CC} - V_{sat}}{R_C + R_E}$$

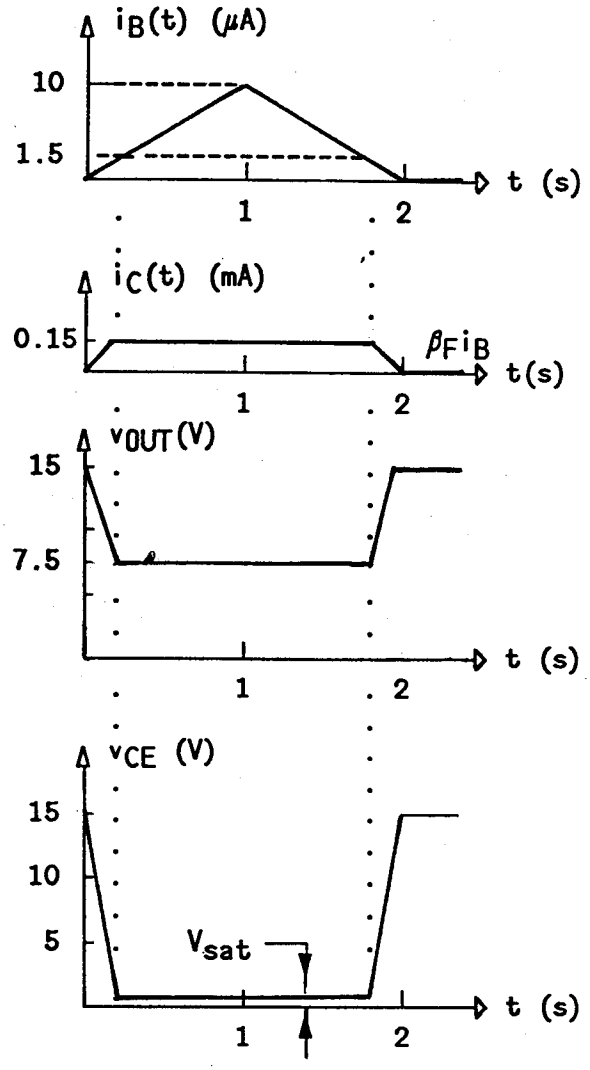
$$= \frac{15\text{ V} - 0.2\text{ V}}{100\text{ k}\Omega} = 0.148\text{ mA} \simeq 0.15\text{ mA}$$

Note that i_C will rise with i_B up to the value 0.15 μA, at which point the BJT will saturate; i_C will remain constant for higher values of i_B. Similarly, v_{OUT} and v_{CE} will fall linearly with i_B until v_{CE} reaches its value of V_{sat}, at which point

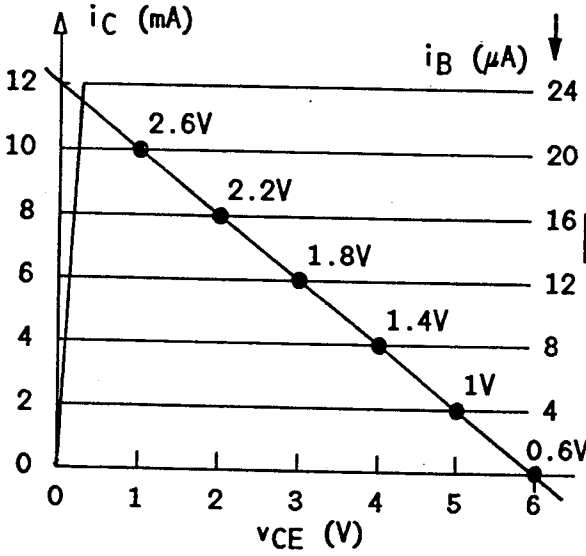
$$v_{OUT} = V_{CC} - i_{C\text{-}sat}R_C$$

$$= 15\text{ V} - (0.15\text{ mA})(50\text{ k}\Omega) = 7.5\text{ V}$$

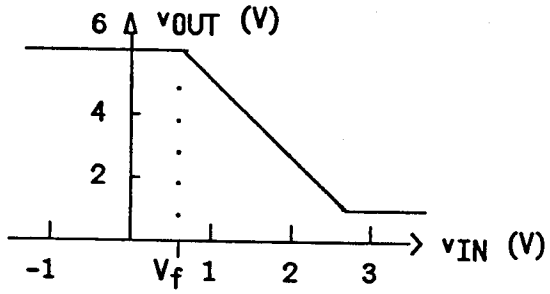
Plots of $v_S(t)$, $i_B(t)$, $i_C(t)$, and the resulting $v_{OUT}(t)$ are shown below.



6.5 The collector and emitter terminals of the BJT are connected directly to the Thevenin circuit formed by V_{CC} and R_C. The load line representing these resistive elements can be plotted directly over the v-i characteristics of the BJT, as shown below. For this load line, $V_{Th} = 6$V and $V_{Th}/R_{Th} = (6\text{ V})/(500\ \Omega) = 12$ mA.



The operating point of the BJT will be determined by the value of i_B. In this case, i_B can be found by plotting the load line of v_{IN} and R_B over the given base-emitter v-i characteristics. Alternatively, this curve can be used to estimate the value of V_f for the base-emitter junction. KVL can then be used to find i_B as a function of v_{IN}. Using the latter method yields $i_B = (v_{IN} - V_f)/R_B$ where, from the figure, $V_f \simeq 0.6$ V. Several operating points, labeled by the v_{IN} value that yields the corresponding i_B, are indicated in the figure above. These points can be used to plot the transfer characteristic of the inverter:



Note that v_{OUT} remains fixed at V_{CC} until v_{IN} exceeds the BJT "threshold" voltage V_f. Similarly, for values of v_{IN} greater than about 2.8 V (i.e., $i_B > 22$ μA), the BJT goes into saturation with $v_{OUT} \simeq 0.25$ V.

6.6 a) The value of β_F can be found by finding the ratio of i_C to i_B at several points in the constant-current region. The v-i curves are evenly spaced, so the value of β_F can be computed anywhere. Along the constant-current portion of the i_B = 24 μA curve, for example, i_C = 12 mA, so that β_F = (12 mA)/(24 μA) = 500.

b) From the base-emitter v-i characteristic, we note that $V_f \simeq 0.6$ V. For a given v_{IN}, the value of i_B can be found by applying KVL to the input loop of the circuit, yielding $i_B = (v_{IN} - V_f)/R_B$. Thus, for v_{IN} = 2.5 V, i_B = (2.5V - 0.6V)/100kΩ = 19 μA. For a β_F of 500, i_C becomes $\beta_F i_B$ = 500(19 μA) = 9.5 mA. Finally, the value of v_{OUT} can be computed by applying KVL to the output loop of the circuit, yielding $v_{OUT} = V_{CC} - i_C R_C$ = 6 V - (9.5 mA)(500 Ω) = 1.25 V. This v_{OUT} is well in excess of the BJT's saturation voltage V_{sat}, indicating that the transistor is not driven to saturation by v_{IN}.

c) If β_F is doubled, the collector current i_C will attempt to increase to the value 1000(19 μA) = 19 mA. If reached, this i_C value would result in a voltage drop across R_C of (19 mA)(500 Ω) = 9.5 V. This unattainable voltage value exceeds the available power supply voltage V_{CC} = 6 V. It would also would require that v_{OUT} somehow drop to a negative value, which it cannot do. We thus conclude that the BJT is driven to

saturation with $v_{OUT} = V_{sat} \simeq 0.25$ V (see Prob 6.5) and $i_{C\text{-}sat} = \frac{V_{CC} - V_{sat}}{R_C} = \frac{6\text{ V} - 0.25\text{ V}}{500\ \Omega} = 11.5$ mA

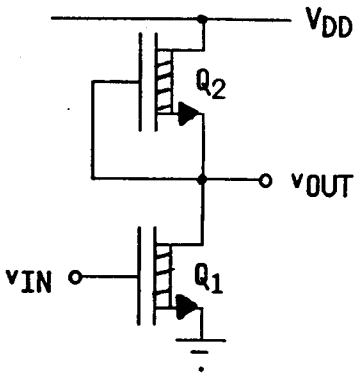
Note that $i_C/i_B \neq \beta_F$ in this case, but the value of i_B, which is determined by KVL taken around the input loop, is still equal to 19 μA.

6.7 The value of i_B for this circuit is given by $i_B = (v_{IN} - V_f)/R_B$ (see Prob. 6.5). If the BJT operates in the constant current region, then i_C will equal $\beta_F i_B$. Meanwhile, $v_{OUT} = V_{CC} - i_C R_C = V_{CC} - \beta_F i_B R_C$, or

$$v_{OUT} = V_{CC} - \frac{\beta_F (v_{IN} - V_f) R_C}{R_B}$$

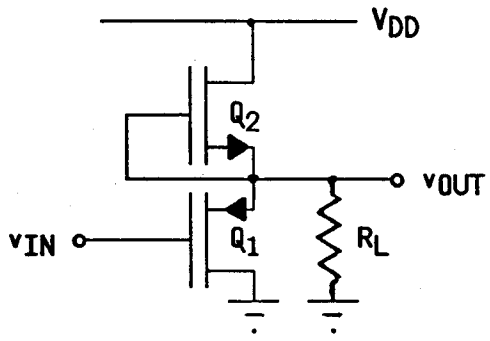
Taking the slope dv_{OUT}/dv_{IN} of this equation yields the voltage "gain" of the circuit, which is equal to $dv_{OUT}/dv_{IN} = -\beta_F R_C/R_B$.

6.8 The transfer characteristic is that of an inverter. The circuit turns on (current begins to flow through the pull-up device) for negative values of v_{IN}. The input device of the inverter must therefore be a depletion-mode MOSFET. Since all devices are to be identical, the upper device must also be a depletion mode MOSFET:



Note that Q_2 has its gate connected to its source, so that $v_{GS2} = 0$. This connection allows i_{D2} to be nonzero for all values of v_{DS2}. The exact value of v_{DS2} is determined by the v_{GS}=0 v-i characteristic of Q_2. The current through Q_2 is set by Q_1.

6.9 The output of the circuit is low when v_{IN} is negative. The output is high (i.e., the input device is in cutoff) for more positive values of v_{IN}. This characteristic can be obtained if a p-channel transistor and n-channel transistor are connected as shown below:



A depletion-mode p-channel device has a positive V_{TR}, yielding a positive turn-on value of v_{IN}. This condition is compatible with the indicated transfer characteristic.

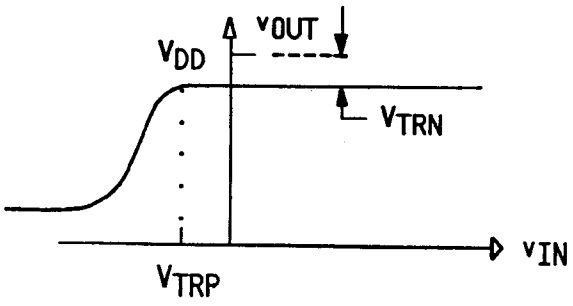
With a p-channel device used as the input transistor, the circuit will

take on complementary form if an n-channel MOSFET is used for the pullup load. The gate of Q_2 is connected to its source, causing Q_2 to operate on its $v_{GS}=0$ v-i characteristic. This connection allows Q_2 to conduct and to pull v_{OUT} up toward V_{DD} when Q_1 goes into cutoff.

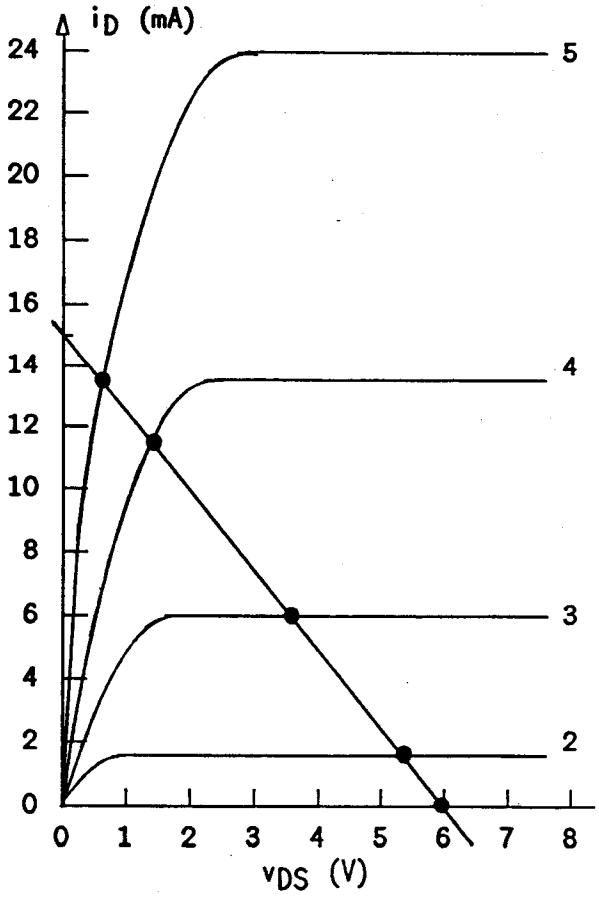
6.10 For this circuit, the n-channel pullup device Q_1, for which $v_{GS1} = v_{DS1}$, obeys the v-i equation

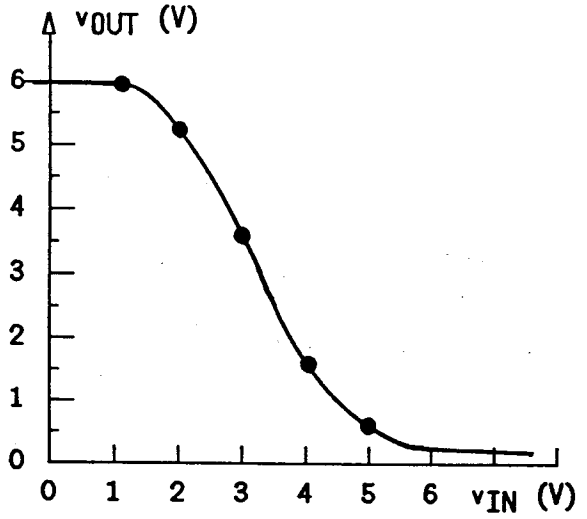
$$i_D = K(V_{DD} - v_{OUT} - V_{TRN})^2.$$

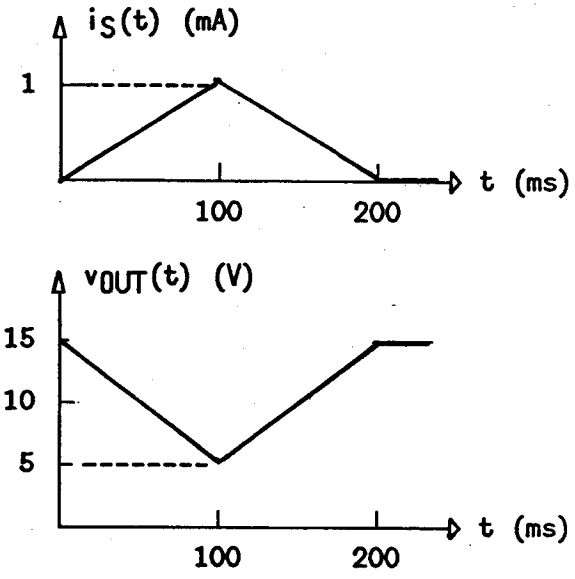
Note that Q_1, with a positive V_{TR}, automatically operates in the constant-current region, since the condition $v_{DS1} > v_{GS1} - V_{TRN}$ will always be met. When v_{IN} is low, the p-channel input device Q_2 is driven into conduction, pulling current through Q_1 and causing v_{OUT} to fall to a small value. Q_2 will conduct as long as v_{IN} is less than V_{TRP}. When v_{IN} is high, Q_2 enters the cutoff state. It would seem that v_{OUT} should rise to the value V_{DD}, but this output can be obtained only if the v_{OUT} terminal drives no load. If the slightest load current is drawn from the v_{OUT} terminal, a v_{GS1} of V_{TRN} is required, causing v_{OUT} to fall to the value $V_{DD} - V_{TRN}$. The transfer characteristic thus has the form shown below.



6.11 The drain and source terminals of the MOSFET are connected directly to the Thevenin circuit formed by V_{DD} and R_D. The load line representing these Thevenin elements can be plotted directly over the v-i characteristic of the MOSFET, as shown below. In this case, $V_{Th} = 6$ V and $V_{Th}/R_{Th} = (6\ V)/(400\ \Omega) = 15$ mA. Several representative operating points, indicated in the figure, are used to construct the accompanying transfer characteristic. Note that v_{OUT} remains fixed at V_{DD} until v_{IN} exceeds the MOSFET threshold voltage $V_{TR} = 1$ V. For v_{IN} greater than about 3.5 V, the MOSFET enters the triode region of operation.







6.12 For a BJT in the active (constant-current) region, $i_C = \beta_F i_B$ and $i_E = (\beta_F + 1) i_B$. If $\beta_F \gg 1$, then $i_E \simeq i_C$. An examination of any one of the horizontal lines on the set of v-i characteristics shows this BJT to have a $\beta_F = i_C/i_B$ of about 100. Clearly, $\beta_F \gg 1$ for this transistor.

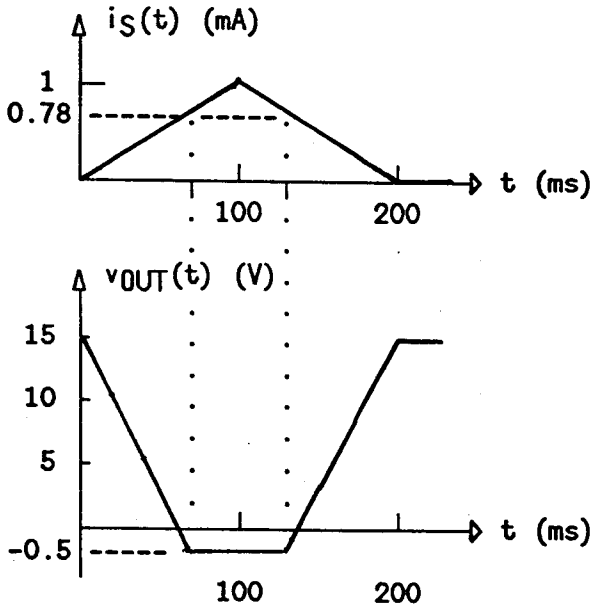
The input current source directly sets i_E (i.e., i_C) to the value i_S. Thus $v_{OUT} = V_{CC} - i_S R_C$. For $i_S = 0$, $v_{OUT} = V_{CC} = 15$ V. For $i_S = 1$ mA (peak value of i_S), $v_{OUT} = 15$ V - (1 mA)(10 kΩ) = 5 V. The value of v_{OUT} will change linearly with i_S for values of i_S between these two extreme limits. A plot of v_{OUT} versus time for the indicated i_S is shown below.

6.13 This problem is similar to Prob. 6.12. In this case, however, the voltage drop across R_C, equal to $i_C R_C$ (essentially equivalent to $i_S R_C$), appears to exceed V_{CC} as i_S heads toward its peak value of 1 mA. In reality, the BJT will be driven out of its constant-current region and into saturation when i_S reaches the value 0.78 mA. This value can be computed by assuming $V_{sat} \simeq 0.2$ V and by noting that the emitter of Q_1 is held at $-V_f \simeq -0.7$V as long as current flows through the base-emitter junction. Q_1 will reach saturation when $v_{CE} = V_{sat}$, i.e. when $v_{OUT} = -V_f + V_{sat} = -0.5$ V. Given that $v_{OUT} = V_{CC} - i_S R_C$ for values of i_S up to the saturation point, the limiting value of i_S becomes [15 V - (-0.5 V)]/(20 kΩ) = 0.78 mA. For larger values of i_S, v_{OUT} will remain fixed at -0.5 V. Further increases in i_S will flow directly via the base-emitter junction of the BJT without extracting an

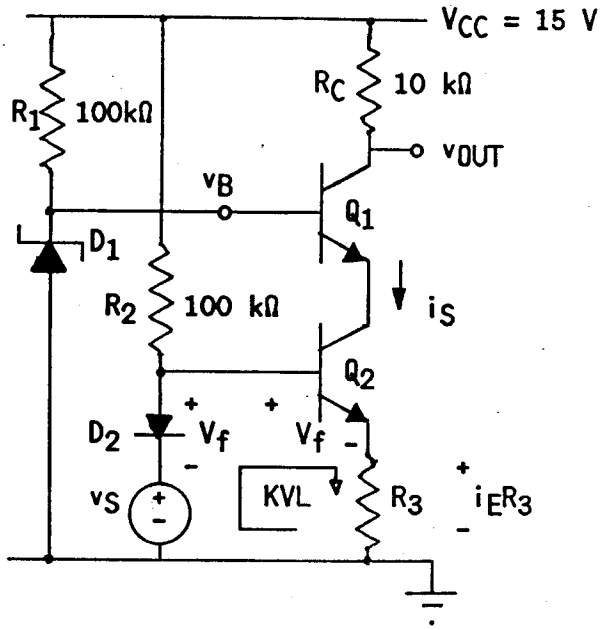
additional current component from i_C. Note that under saturation conditions, $i_C \neq \beta_F i_B$.

It is also interesting to note the nature of the i_S current source. If truly ideal, this source will adjust the voltage across its terminals to meet the constraints of its load. Thus, the top terminal of the i_S source will be held at the value $-V_f$ relative to ground for all values of i_S greater than zero.

Here is a plot of v_{OUT} versus i_S:



6.14 Many designs will accomplish the desired task. Here is one design that utilizes a second BJT:



In this circuit, the large resistance R_2 forward-biases D_2 by forcing a small current through the diode and into the v_S source. The voltage drop across D_2, which is approximately equal to V_f, is used to overcome the base-emitter voltage drop of Q_2. Applying KVL to the base loop of Q_2 yields

from D_2 | from Q_2

$$-v_S - V_f + V_f + i_E R_3 = 0$$

$\Longrightarrow i_E = v_S/R_3$. For large β_F, $i_S \simeq i_E = v_S/R_3$.

The purpose of the zener D_1 is to provide a voltage above ground for the base terminal of Q_1. D_1 is forced into its reverse-breakdown region by R_1, so that $v_B = V_{ZK}$. Without the zener in place, the base of Q_1 would be held at ground, forcing the voltage of the emitter of Q_1 to the value $-V_f$. This condition would also require that the collector of Q_2 be held at $-V_f$ relative to ground. Since ground (0 V) is the lowest voltage in the circuit, this

condition cannot be met. Including the zener D_1 eliminates the problem.

Recall that V_P of the n-channel JFETs has a negative value.

6.15 The first step is the computation of the current i_{D2} as a function of v_{IN}. An examination of Q_2 reveals that $v_{GS2} = v_{IN}$. If Q_2 operates in its constant-current region, then

$$i_{D2} = (I_{DSS}/V_P^2)(v_{GS2} - V_P)^2$$
$$\equiv K(v_{IN} - V_P)^2$$

where the equivalent JFET parameter $K = I_{DSS}/V_P^2$ has been substituted.

For gate currents into the JFETs of zero, it follows that $i_{D1} = i_{D2}$. If Q_2 operates in its constant-current region, it follows that

$$v_{OUT} = V_{CC} - i_{D2}R_D$$
$$= V_{CC} - KR_D(v_{IN} - V_P)^2$$

The above analysis assumes both JFETs to operate in the constant current region. Device Q_2 will do so for

$$v_{DS2} > v_{GS2} - V_P$$

Since $v_{DS2} = -v_{GS1}$, this condition becomes

$$-v_{GS1} > v_{GS2} - V_P$$

If Q_1 also operates in the constant-current region, then v_{GS1} will equal v_{GS2} for matched devices, as noted above. Under such conditions, the constant-current condition on Q_2 can be expressed as

$$-v_{GS2} > v_{GS2} - V_P,$$

or $$v_{GS2} < V_P/2$$

With $v_{GS2} = v_{IN}$, this condition becomes $v_{IN} < V_P/2$.

The above analysis assumes Q_1 to operate in the constant-current region. It will do so if

$$v_{DS1} > v_{GS1} - V_P$$

or

$$v_{OUT} + v_{GS1} > v_{GS1} - V_P$$

$$\Longrightarrow \quad v_{OUT} > -V_P$$

6.16 a) Q_1 will operate in the constant current region if $v_{DS1} > v_{GS1} - V_{TR1}$. For this circuit, $v_{DS1} = v_{OUT}$, so that the above condition becomes $v_{OUT} > v_{GS1} - V_{TR1} = 2\text{ V} - 1\text{ V} = 1\text{ V}$. In the above equation, the bias value of v_1 has been substituted for v_{GS1}.

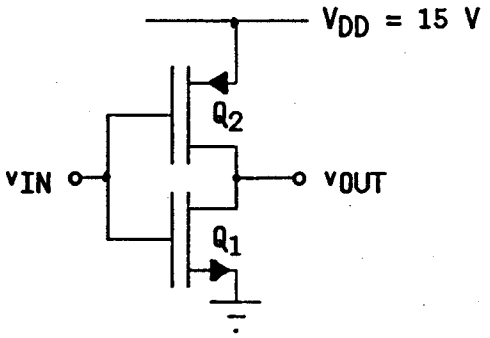
b) Similarly, Q_2, the p-channel device, will operate in the constant-current region for $v_{DS2} < v_{GS2} - V_{TR2}$. The bias value of v_{GS2} is equal to $V_2 - V_{DD}$, and $v_{DS2} = v_{OUT} - V_{DD}$. The constant-current region condition thus becomes

$$v_{OUT} - V_{DD} < V_2 - V_{DD} - V_{TR2}, \text{ or}$$
$$v_{OUT} < V_2 - V_{TR2} = 11\text{V} - (-2\text{V}) = 13\text{ V}$$

Both devices will operate in the constant-current region for

$$1\text{ V} < v_{OUT} < 13\text{ V}.$$

6.17 Here is a diagram of the circuit described in the problem:



For $v_{IN} > V_{TRN}$, v_{GS1} will exceed the threshold voltage of Q_1, causing the n-channel device to conduct and v_{OUT} to be forced toward ground. Over this region of operation, Q_2 will function as the pullup load to Q_1.

For $v_{IN} - V_{DD} < V_{TRP}$, Q_2 will conduct, forcing v_{OUT} toward V_{DD}. Note that V_{TRP} has a negative value. Over this region of operation, Q_1 will function as the pulldown load to Q_2. Here is a qualitative sketch of the resulting transfer characteristic: