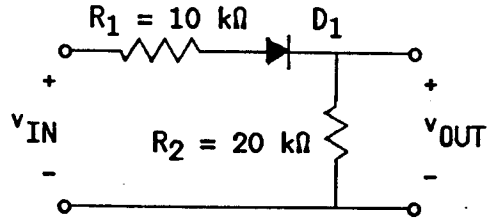
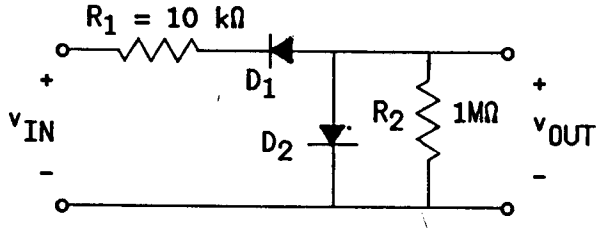
Chapter 4
Circuit Containing Two-Terminal Nonlinear Devices

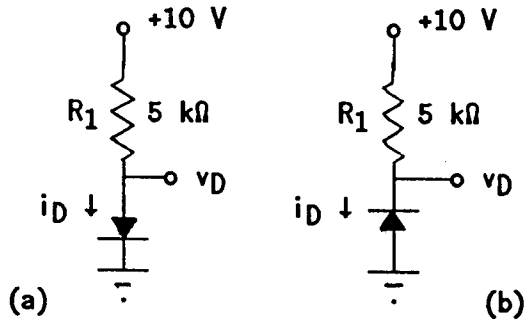
4.1 Draw the v_{IN}-v_{OUT} transfer characteristic of the diode circuit shown below. D_1 has a turn-on voltage of $V_f = 0.5$ V.



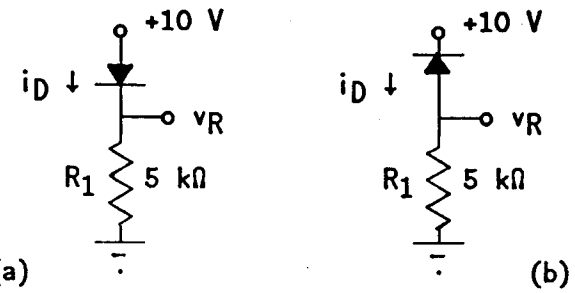
4.2 Draw the v_{IN}-v_{OUT} transfer characteristic of the diode circuit shown below. D_1 and D_2 have turn-on voltages of $V_f = 0.6$ V.



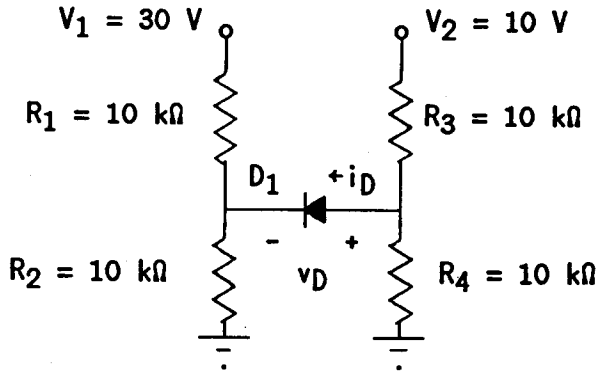
4.3 Find the diode voltage and current in the following circuits. For each diode, $V_f = 0.5$ V.



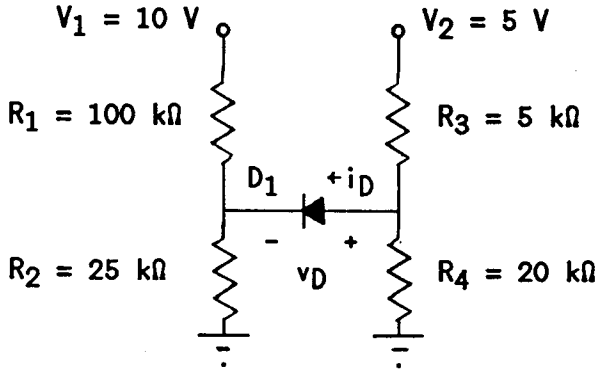
4.4 Find i_D and v_R in the following circuits. For each diode, $V_f = 0.5$ V.



4.5 Find the diode voltage and current in the following circuit. D_1 has a turn-on voltage of $V_f = 0.5$ V.



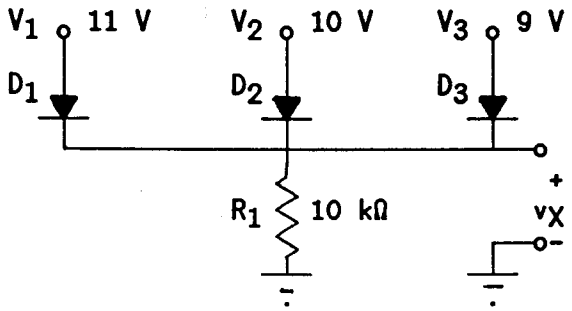
4.6 Find the diode voltage and current in the following circuit. D_1 has a turn-on voltage of $V_f = 0.5$ V.



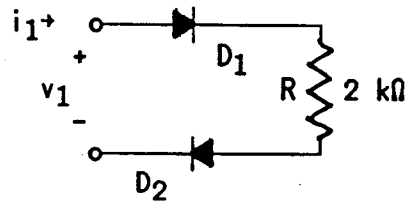
4.7 Find v_D and i_D in the circuit of Prob. 4.6 if $V_1 = -10$ V.

4.8 Find v_D and i_D in the circuit of Prob. 4.6 if $V_2 = 50$ V.

4.9 Find the voltage v_X in the following circuit if $V_f = 0.7$ V for each diode:

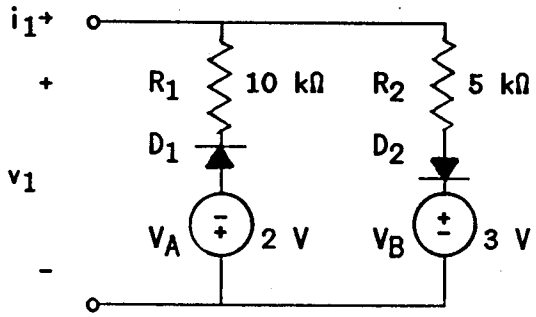


4.10 Plot i_1 versus v_1 for the circuit shown below if each diode has a V_f of 0.6 V:

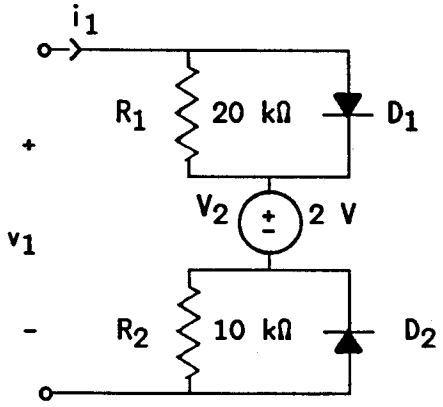


4.11 Repeat Prob. 4.10 if the direction of D_2 is reversed.

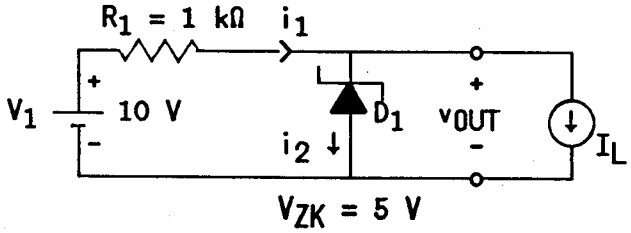
4.12 Plot i_1 versus v_1 for the circuit shown below if each diode has a V_f of 0.6 V:



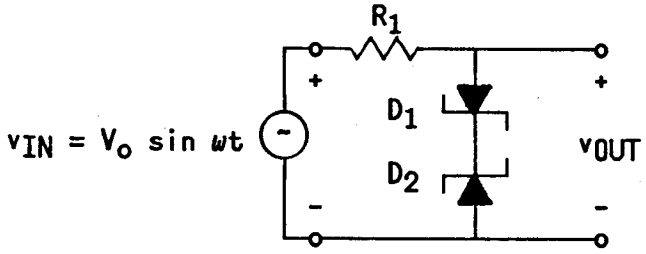
4.13 Plot the i-v relation of the circuit shown below if each diode has a turn-on voltage of $V_f = 0.6$ V:



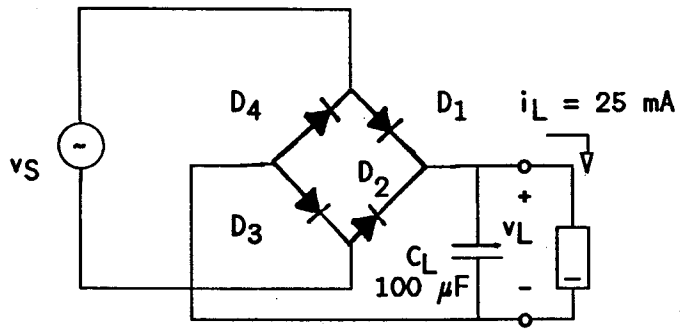
4.14 In the zener circuit shown below, the "load" consists of a current source of value I_L. Over what range of I_L will the zener be in reverse breakdown? Over what range of I_L will the zener become forward biased?



4.15 Two identical zener diodes with V_{ZK} = 3.3 V and V_f = 0.7 V are connected "back-to-back", as shown. Plot v_{OUT} versus time for V_o = 1 V, 5 V, and 10 V.



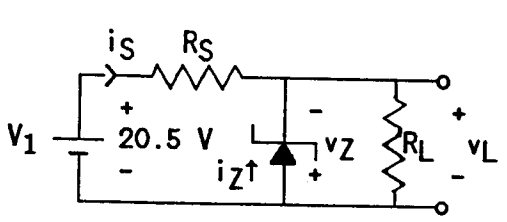
4.16 The full-wave bridge rectifier shown below is used to drive a nonlinear load which draws a *constant current* of 25 mA. For each diode, V_f = 0.7 V. The sinusoidal source v_S has a peak value of 46.4 V and a frequency of 60 Hz.

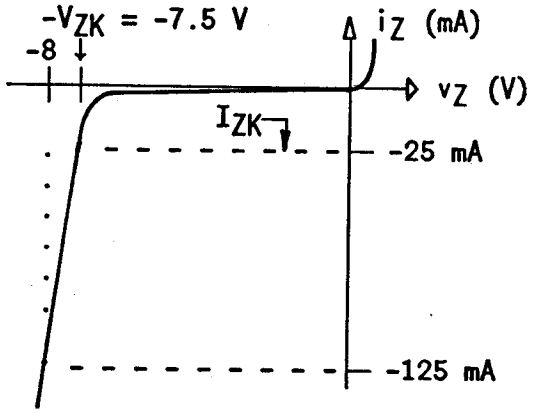


$v_S = V_o \sin \omega t$

a) What is the peak value of v_L?
b) What is the frequency of the ripple component of v_L?
c) Estimate the peak-to-peak value of the ripple component of v_L.
d) What is the average (dc) value of v_L?
e) What is the time-average power dissipated in the load?

4.17 A 1-W zener diode with the v-i characteristic shown below is connected to a resistive circuit.

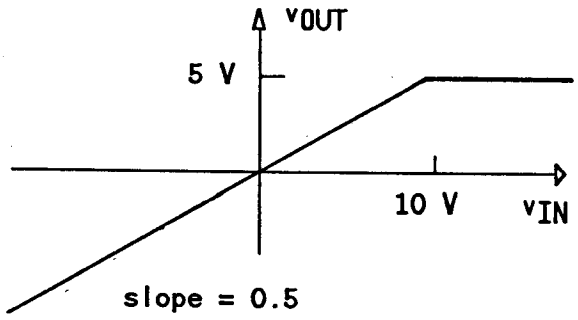




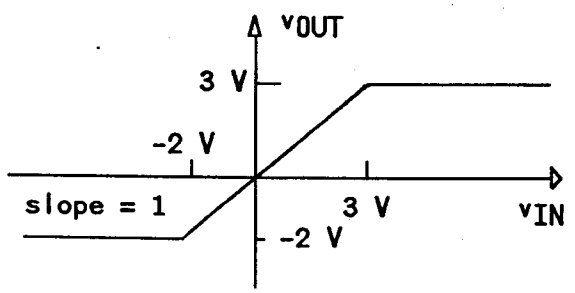
a) With R_L disconnected, find the value of R_S which will cause the maximum allowed power to be dissipated in the zener.

b) When R_S = 200 Ω and R_L is disconnected from the circuit, the zener voltage is -7.8 V. The load resistance R_L is now connected. Find the smallest value that R_L can have if the reverse-breakdown zener current is to be at least I_{ZK}.

4.18 Using any components you wish, design a circuit that has the following transfer characteristic:



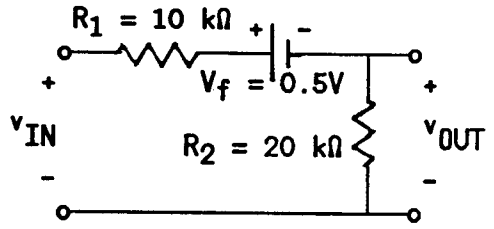
4.19 Design a limiter circuit that has the following voltage transfer characteristic:



Chapter 4

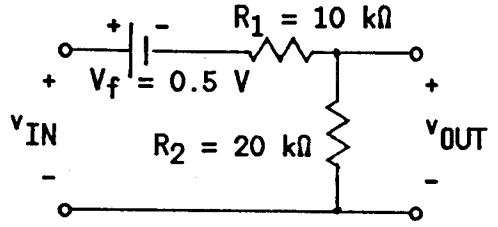
Solutions

4.1 For $v_{IN} > V_f$, D_1 will become forward biased. Substitution of an appropriate piecewise linear model under these conditions leads to:



The resistance r_d of the diode's piecewise linear model is assumed to be much less than R_1 and R_2, and is omitted from the model.

The order of the series connection of R_1 and V_f can be reversed, yielding the following circuit:

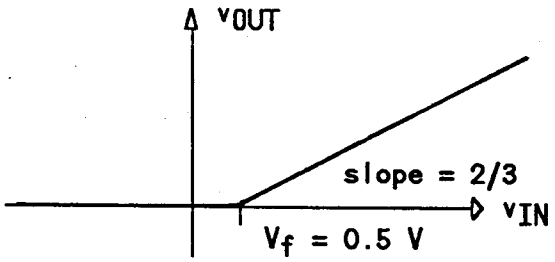


The output v_{OUT} can be found in this latter version of the circuit using voltage division:

$$v_{OUT} = (v_{IN} - V_f)\frac{R_2}{R_1 + R_2} = \frac{2}{3}(v_{IN} - V_f)$$

For $v_{IN} < V_f$, D_1 ceases to conduct, effectively disconnecting R_2 from the circuit. Under these conditions, $v_{OUT} = 0$.

The transfer characteristic of the circuit over the complete range of v_{IN} is shown below.

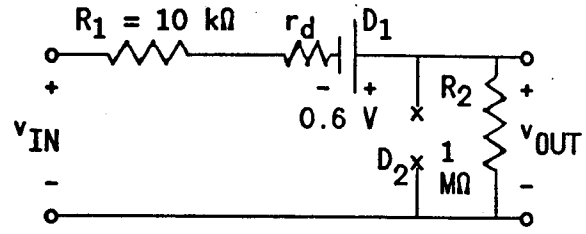


4.2 For $v_{IN} < -V_f$, D_1 becomes forward biased and D_2 reverse biased. An appropriate piecewise linear model for this set of conditions is shown below. The value of r_d is assumed to be negligible, so that

$$v_{OUT} = \frac{R_2}{R_1 + R_2}(v_{IN} + V_f)$$

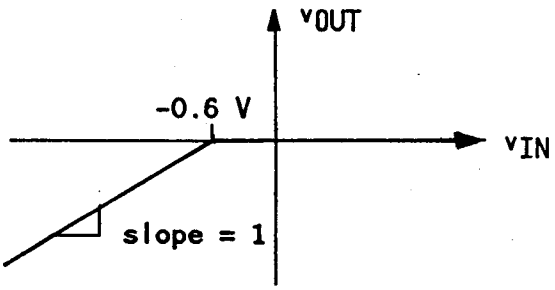
$$= \frac{1\ M\Omega}{10\ k\Omega + 1\ M\Omega}(v_{IN} + V_f)$$

$$\simeq (v_{IN} + V_f)$$



For $v_{IN} > -V_f$, D_1 becomes reverse biased, effectively disconnecting the v_{OUT} terminals from the rest of the circuit. Under these conditions, $v_{OUT} = 0$. Note that D_2 is not forward biased for any value of v_{IN}.

The transfer characteristic of the circuit over the complete range of v_{IN} is shown below.



4.3 a) The 10-V voltage bus is of the proper polarity to forward bias the diode. Assume this condition to be true, so that $v_D = V_f = 0.5$ V. Application of KVL from the voltage bus to ground yields

$$i_D R_1 + v_D = 10\ V$$

or

$$i_D = \frac{10\ V - 0.5\ V}{5\ k\Omega} = 1.9\ mA$$

This current flows in the forward-bias direction through the diode. The original assumption of forward-bias operation is correct.

b) In this case the voltage bus reverse biases the diode, so that

$i_D = 0$. Since no current flows through R_1, the voltage drop across it is zero, and $v_D = 10$ V.

4.4 a) The voltage bus is of the proper polarity to forward bias the diode. Assume this condition to be true, so that $v_D = V_f = 0.5$ V. Application of KVL from the voltage bus to ground yields

$$v_R = 10 \text{ V} - v_D = 9.5 \text{ V}$$

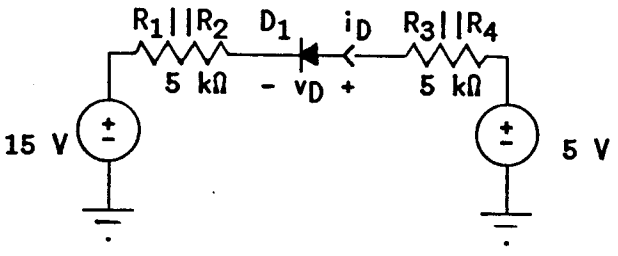
where

$$i_D = \frac{v_R}{R_1} = \frac{9.5 \text{ V}}{5 \text{ k}\Omega} = 1.9 \text{ mA}$$

This current flows in the forward bias direction through the diode, confirming the original assumption of forward-bias operation.

b) In this case, the voltage bus reverse-biases the diode, so that $i_D = 0$. Since no current flows through R_1, the voltage drop across it is zero, and $v_R = 0$.

4.5 Find the Thevenin equivalent of the resistive circuit on either side of the diode:

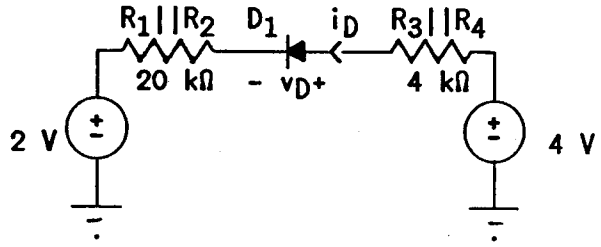


In this equivalent circuit, the voltage on the right side tends to forward bias D_1, while the voltage on the left side tends to reverse bias D_1. The latter voltage is larger, hence D_1 becomes reverse biased with $i_D = 0$ and v_D negative. The voltage v_D is equal to the open-circuit voltage on the right side of the diode minus the open-circuit voltage on the left side:

$$v_D = 5 \text{ V} - 15 \text{ V} = -10 \text{ V}$$

In this circuit, the drops across the Thevenin resistances $R_1||R_2$ and $R_3||R_4$ are zero because the currents flowing through them are zero.

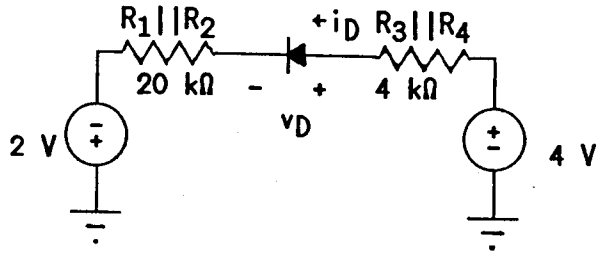
4.6 Find the Thevenin equivalent of the resistive circuit on either side of the diode:



In this equivalent circuit, the voltage on the right side tends to forward bias D_1, while the voltage on the left side tends to reverse bias D_1. The former voltage is larger, hence D_1 becomes forward biased with $v_D = V_f = 0.5$ V and i_D positive. KVL taken around the loops yields

$$i_D = \frac{4 \text{ V} - 0.5 \text{ V} - 2 \text{ V}}{20 \text{ k}\Omega + 4 \text{ k}\Omega} = 62.5 \ \mu\text{A}$$

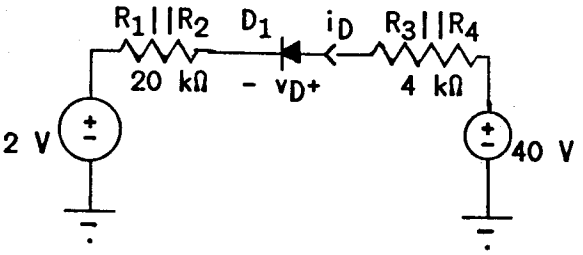
4.7 Forming the Thevenin equivalent of both sides of the circuit results in the following:



In this case, both Thevenin voltages act to forward bias the diode. KVL taken around the loop yields

$$i_D = \frac{4\text{ V} - 0.5\text{ V} - (-2\text{ V})}{20\text{ k}\Omega + 4\text{ k}\Omega} = 0.23\text{ mA}$$

4.8 Forming the Thevenin equivalent of both sides of the circuit results in the following alternative representation of the circuit:



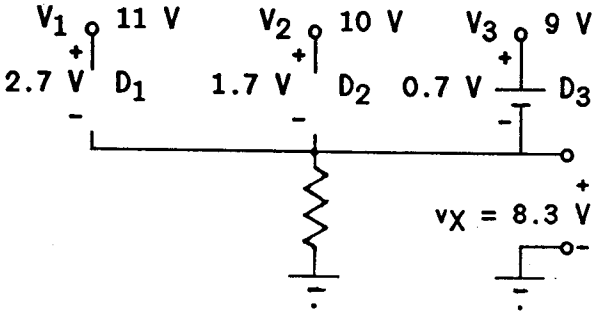
In this case the voltage on the right side of the diode is larger than the voltage on the left side; D_1 becomes forward biased with $v_D = 0.5$ V and

$$i_D = \frac{40\text{ V} - 0.5\text{ V} - 2\text{ V}}{20\text{ k}\Omega + 4\text{ k}\Omega} = 1.56\text{ mA}$$

4.9 Each of the indicated voltage sources will tend to forward bias the diode to which it is connected. Only one source will actually forward bias its diode, however. If a diode is forward biased, then v_X will be driven to the voltage $V_n - V_f$, where V_n is the voltage behind the diode that is turned on. Since all three V_n are different, an inconsistency will exist if more than one diode is turned on.

One method of determining which diode is forward biased involves the "guessing" technique. Specifically, the circuit is examined with one diode assumed turned on. An inconsistency will result if the wrong diode is chosen.

With D_3 assumed on, for example, the circuit can be modeled by substituting a voltage source V_f for D_3 and open circuits for D_1 and D_3:



By KVL, $v_X = V_3 - V_f = 9\text{ V} - 0.7\text{ V} = 8.3\text{ V}$. This condition would appear to result in diode voltages

$v_{D1} = V_1 - v_X = 11\text{ V} - 8.3\text{ V} = 2.7\text{ V}$

$v_{D2} = V_2 - v_X = 10\text{ V} - 8.3\text{ V} = 1.7\text{ V}$

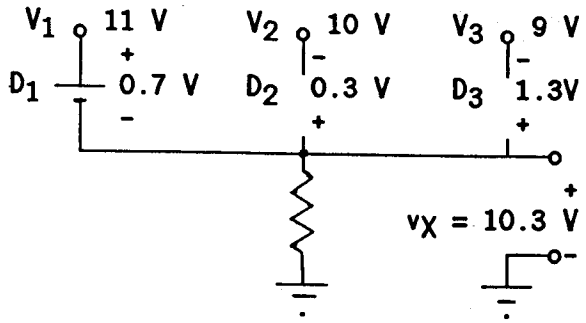
across D_1 and D_2, respectively. These results are inconsistent with the properties of the diodes, for which the voltage can be no more than V_f under forward-biased conditions. The inconsistency shows that D_3 cannot be the forward-biased diode.

Selecting D_2 as the forward-biased diode ($v_X = 9.3$ V) produces an equally impossible result:

$$v_{D1} = 11\text{ V} - 9.3\text{ V} = 1.7\text{ V}$$

Choosing D_1 as the forward-biased diode results in the correct solution:

$$v_X = V_1 - V_f = 10.3\text{ V}$$



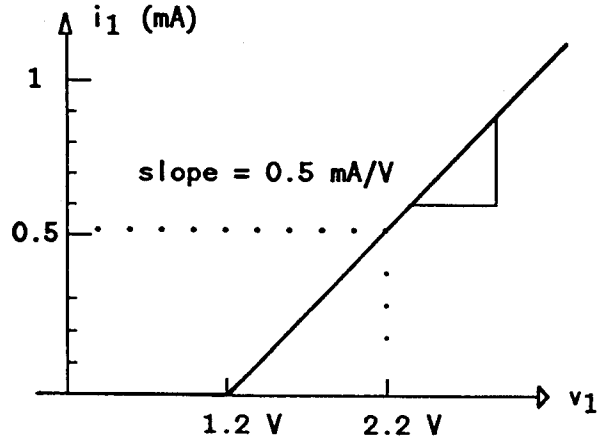
With D_1 forward biased, diodes D_2 and D_3 are reverse-biased by voltages of 0.3 V and 1.3 V, respectively. These conditions are consistent with the properties of the diodes. V_1, which is the strongest of the three sources, forward biases its diode, thereby forcing the other diodes into reverse bias.

4.10 For $v_1 > 2V_f$, both diodes will be turned on (forward biased) with $v_D = V_f = 0.6$ V. Application of KVL results in

$$i_1 = \frac{v_1 - 2V_f}{R} = (0.5 \text{ mA/V})v_1 - 0.6 \text{ mA}$$

where $1/R = 0.5$ mA/V.

For $v_1 < 2V_f$, both diodes will be turned off, so that $i_1 = 0$. Here is a plot of i_1 vs. v_1 for this circuit:



4.11 If the direction of D_2 is reversed, current can flow through the circuit in neither direction; i_1 will be zero for all values of v_1.

4.12 For $v_1 > 3.6$ V, D_2 will conduct with $v_{D2} = V_f = 0.6$ V, and

$$i_1 = \frac{v_1 - V_B - V_f}{R_2}$$

$$= (0.2 \text{ mA/V})\, v_1 - 0.72 \text{ mA}$$

where $1/R_2 = 0.2$ mA/V.

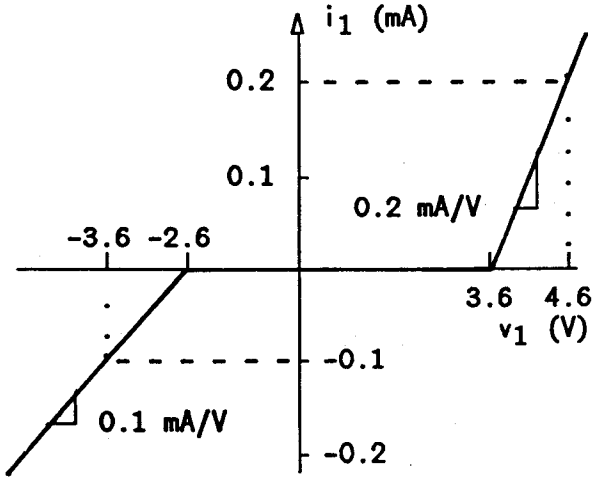
For $v_2 < -2.6$ V, D_1 will conduct with $v_{D1} = V_f = 0.6$ V, and

$$i_1 = \frac{v_1 + V_A + V_f}{R_2}$$

$$= (0.1 \text{ mA/V})\, v_1 + 0.26 \text{ mA}$$

where $1/R_1 = 0.1$ mA/V. Note that i_1 will be negative in this case.

For -2.6 V $< v_1 < 3.6$ V, neither D_1 nor D_2 will conduct, so that $i_1 = 0$. Here is a plot of i_1 versus v_1 for both positive and negative v_1:



4.13 Consider the circuit with neither diode forward biased (both diodes set to open circuits). Under such conditions, the current becomes

$$i_1 = \frac{v_1 - V_2}{R_1 + R_2} = 33.3\ \mu A/V\ (v_1 - V_2)$$

where $1/(R_1 + R_2) = 33.3 \mu A/V$. The current i_1 equals zero at $v_1 = V_2 = 2$ V.

When i_1 becomes so positive that the drop across R_1 reaches $V_f = 0.6$ V, D_1 will become forward biased. This condition occurs at

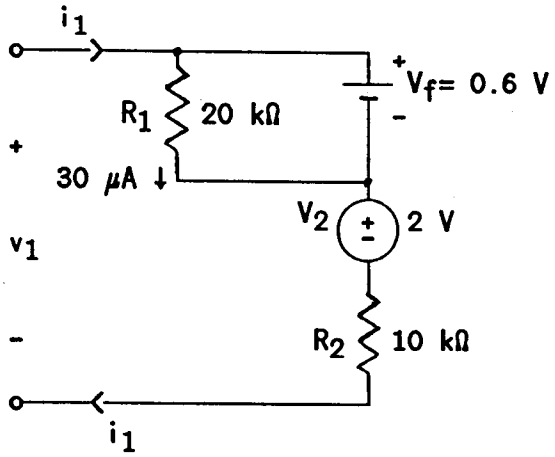
$i_1 = V_f/R_1 = (0.6\ V)/(20\ k\Omega) = 30\ \mu A$;

$v_1 = i_1R_1 + V_2 + i_1R_2$

$= (30\mu A)(20k\Omega) + 2\ V + (30\mu A)(10k\Omega)$

$= 0.6\ V + 2\ V + 0.3\ V = 2.9\ V.$

Further increases in v_1 will keep D_1 forward biased. Substituting an appropriate piecewise linear model under these conditions results in



For this equivalent circuit,

$$i_1 = \frac{v_1 - (V_f + V_2)}{R_2}$$

$$= (100\ \mu A/V)\ v_1 - 260\ \mu A$$

where $1/R_2 = 100\ \mu A/V$. Note that, with D_1 forward biased, the incremental slope of i_1 versus v_1 increases from $1/(R_1 + R_2) = 33.3\ \mu A/V$ to $1/R_2 = 100\ \mu A/V$, since R_1 is now bypassed by the forward-biased D_1. The current through R_1 remains fixed at $V_f/R_1 = 30\ \mu A$. Any increase in i_1 beyond this value must flow through D_1.

Now consider the circuit for decreasing v_1. As v_1 falls below 2 V, V_2 will begin to drive current in the negative direction. When i_1 becomes so negative that the drop across R_2 reaches $-V_f = -0.6$ V, D_2 will become forward biased. This condition occurs for $i_1 = \frac{-V_f}{R_2} = \frac{-0.6\ V}{10\ k\Omega} = -60\ \mu A$ and

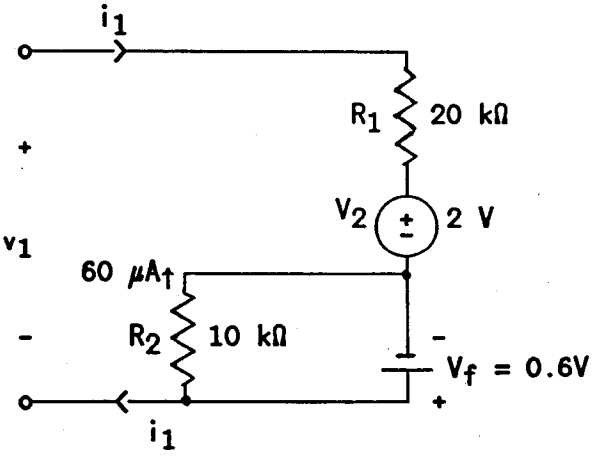
$v_1 = i_1R_1 + V_2 + i_1R_2$

$= (-60\mu A)(20k\Omega) + 2\ V + (-60\mu A)(10k\Omega)$

$= -1.2\ V + 2\ V - 0.6\ V = 0.2\ V$

Further decreases in v_1 will keep D_2 forward biased. Note that V_2 forward biases D_2 while v_1 is still positive but less than 2 V.

Substituting an appropriate piecewise linear model for D_2 under these conditions results in



For this equivalent circuit,

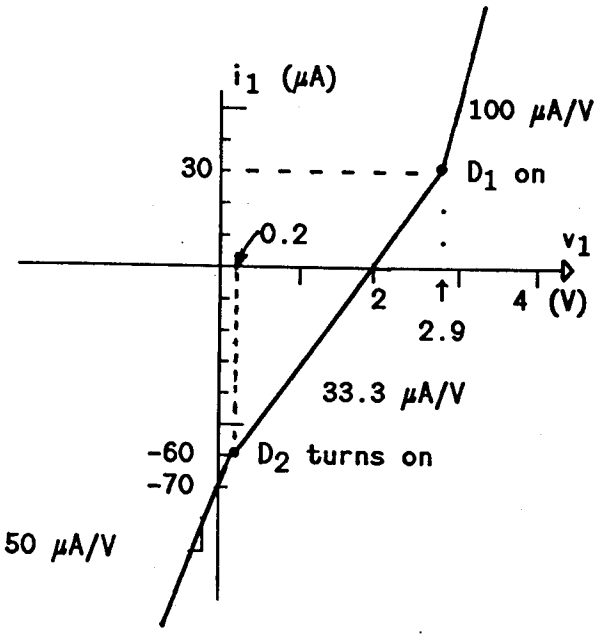
$$i_1 = \frac{v_1 - V_2 + V_f}{R_1}$$

$$= (50\ \mu A/V)\ v_1 - 70\ \mu A$$

where $1/R_1 = 50\ \mu A/V$. Note that the incremental slope of i_1 versus v_1 increases from $1/(R_1 + R_2) = 33.3\ \mu A/V$ to $1/R_1 = 50\ \mu A/V$ when D_2 becomes

forward biased, since R_2 is bypassed by the forward-biased D_2.

Here is a plot of i_1 versus v_1 for the full range of v_1:



4.14 The polarity of V_1 is such that it will tend to force D_1 into reverse breakdown. The latter condition will be established if the reverse current i_2 into the zener remains positive. If the zener is assumed to be in reverse breakdown, with $v_{OUT} = V_{ZK}$, i_1 will be given by

$$i_1 = \frac{V_1 - V_{ZK}}{R_1} = \frac{10\text{ V} - 5\text{ V}}{1\text{ k}\Omega} = 5\text{ mA}$$

From KCL, the reverse current i_2 becomes $i_2 = i_1 - I_L$. This current will be positive, with the zener in reverse breakdown, for $I_L < 5$ mA. If I_L exceeds this critical value, i_2 will go to zero, and i_1 will equal i_L. Under these conditions, the output will become

$$v_{OUT} = V_1 - I_L R_1$$

A plot of this equation over the appropriate range of I_L will be a straight line.

If I_L becomes too large, v_{OUT} will become negative and will forward bias D_1. This latter condition occurs for

$$V_1 - I_L R_1 = -V_f$$

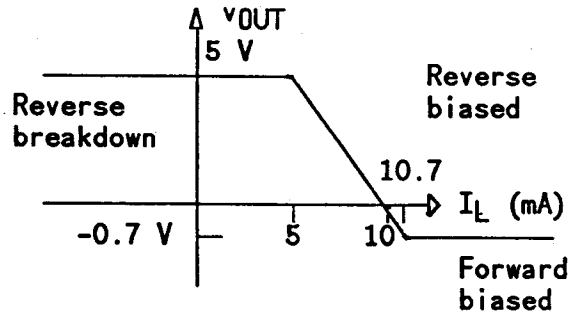
or

$$I_L = \frac{V_1 + V_f}{R_1} = \frac{10\text{ V} + 0.7\text{ V}}{1\text{ k}\Omega} = 10.7\text{ mA}$$

where the value $V_f = 0.7$ V has been assumed. Under these conditions, i_1 remains fixed at

$$\frac{V_1 + V_f}{R_1} = 10.7\text{ mA}$$

for further increases in I_L. If I_L increases above 10.7 mA, the additional current component will flow through the forward-biased diode D_1. Here is a plot of v_{OUT} versus I_L:



4.15 When the instantaneous positive value of v_{IN} exceeds

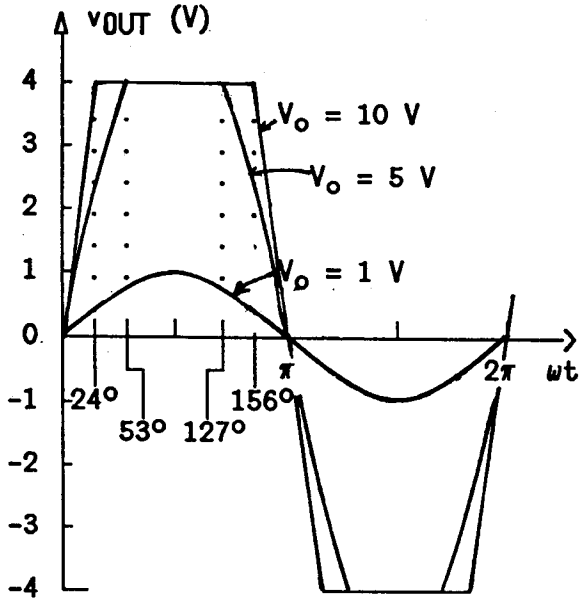
$V_{ZK} + V_f = 3.3\text{ V} + 0.7\text{ V} = 4\text{ V}$,

D_1 will become forward biased and D_2 will go into reverse breakdown. Under these conditions, v_{OUT} will be clamped to the value 4 V.

Conversely, when v_{IN} becomes more negative than $-(V_{ZK} + V_f) = -4$ V, D_2 will become forward biased and D_1 will go into reverse breakdown. Under these latter conditions, v_{OUT}

will be clamped to the value -4 V. For values of v_{IN} between these limits, either D_1 or D_2 will be reverse biased (open circuit), so that $v_{OUT} = v_{IN}$. Note that the value of R_1 does not affect the output of the circuit provided that it is much larger than the incremental reverse-breakdown resistance r_z of either zener. Under such conditions, r_z may be neglected.

Here is a plot of v_{OUT} versus time for the specified values of V_o:



4.16 a) The peak load voltage will be two V_f drops below the peak value of v_S, i.e. $|v_L|_{peak} = 46.4\text{ V} - 1.4\text{ V} = 45\text{ V}$.

b) The four diodes form a full-wave rectifier. Both the positive and negative peaks of v_S will result in a positive peak being applied to C_L. The ripple component will thus have a frequency of 120 Hz, i.e. twice that of v_S.

c) After being recharged to a peak voltage of 45 V, the capacitor will be discharged by the constant load current according to the equation

$$\frac{dv_C}{dt} = \frac{i_L}{C_L} = \frac{-25\text{ mA}}{100\ \mu\text{F}} = -0.25\text{ V/ms}$$

Unlike the exponential voltage decay experienced with a resistive load, the discharge of C_L under constant load-current conditions proceeds at a constant rate. Under full-wave rectification conditions, the discharge of the capacitor will continue for approximately 1/120 second (one period of the ripple), so that $dt \simeq 8.3$ ms, and

$dv_L = (-0.25\text{ V/ms})(8.3\text{ ms}) \simeq -2.08\text{ V}$

This dv_L represents the peak-to-peak ripple component of v_L.

d) Since the ripple component of v_L is a symmetrical ramp-like voltage (C_L discharges at a constant rate between recharge peaks), the average value of the total v_L becomes

$$|v_L|_{peak} - \frac{|v_{rip}|}{2} = 45\text{V} - 1.04\text{ V} \simeq 44\text{ V}$$

e) The time average power dissipated in the load becomes

$$\langle i_L v_L \rangle = (25\text{ mA})(44\text{ V}) = 1.1\text{ W}$$

The brackets $\langle\rangle$ denote time-average quantity.

4.17 a) With $V_1 > V_{ZK}$ and R_L disconnected, the zener will be forced into reverse breakdown. Under this condition, all of the current through R_S will flow in the reverse-breakdown direction through the zener. The maximum permissible value of this current is determined by the 1-W power limitation:

$$p_Z = v_Z i_Z = 1\text{ W}$$

$\Longrightarrow$ $i_Z = p_Z/v_Z = (1\ W)/(-8\ V) =$ -125 mA maximum. Application of KVL results in the equation

$$i_S = \frac{V_1 + v_Z}{R_S}$$

A current of i_S = 125 mA (i_Z = -125 mA) will flow for

$$R_S = \frac{V_1 + v_Z}{i_S} = \frac{20.5\ V - 8\ V}{0.125\ A} = 100\ \Omega$$

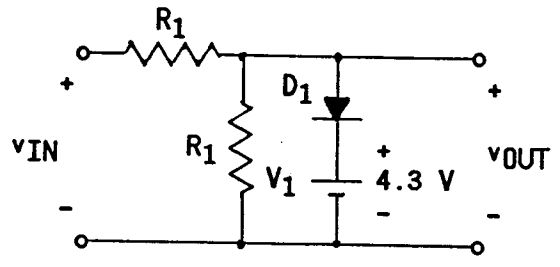
b) The fact that v_Z = -7.8 with R_S = 200 Ω and R_L disconnected is really irrelevant to the problem. What must be examined are the conditions under which v_Z will be reduced to its "knee" value of $-V_{ZK}$ = -7.5 V. When this condition occurs, i_S will be equal to

$$\frac{V_1 - V_{ZK}}{R_S} = \frac{20.5\ V - 7.5\ V}{200\ \Omega} = 65\ mA$$

and v_L will equal 7.5 V. If i_Z = -25 mA ("knee" current), then 25 mA will flow in the reverse-breakdown direction into the zener, leaving 40 mA to flow into R_L. The value of R_L that will yield these conditions can now be computed:

$$R_L = 7.5\ V/40\ mA = 187.5\ \Omega$$

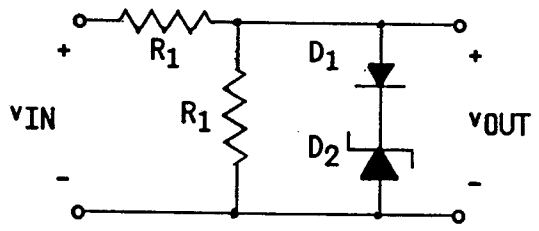
4.18 Here is one circuit that will provide the required transfer characteristic:



For $v_{IN} > V_1 + V_f$, the diode will conduct and clamp v_{OUT} to the value $V_1 + V_f$. The desired value of this latter voltage is 5 V. Hence the voltage source V_1 should be set to the value 5 V - V_f. For a V_f of 0.7 V, the required value of V_1 becomes 4.3 V. For $v_{IN} < V_1 + V_f$, the diode ceases to conduct (open circuit) and, via voltage division, $v_{OUT} = v_{IN}/2$.

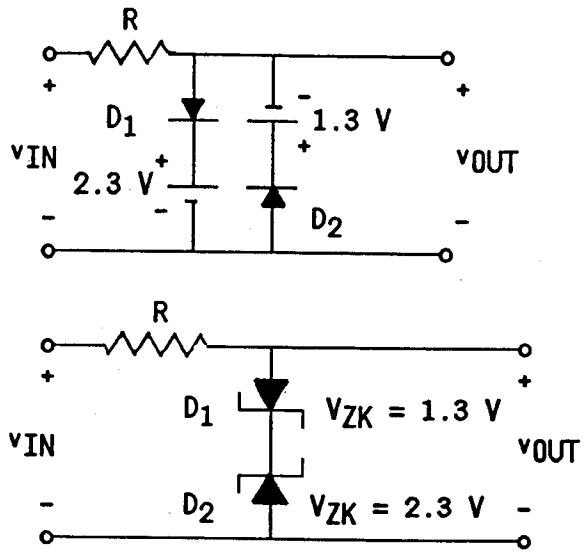
The value of R_1 is not critical, but it must be small enough to provide sufficient forward-bias current when D_1 conducts. Conversely, R_1 much be much larger than the piecewise-linear resistance of D_1 under forward-biased conditions. If R_1 is too small, the latter resistance must be taken into account.

Here is an alternative version of the circuit that uses a zener instead of the dc voltage source V_1. Other solutions are also possible.



V_{ZK} = 4.3 V V_f = 0.6 V

4.19 The transfer characteristic can be realized by a circuit in which the output is clamped in both the positive and negative directions. The following two circuits will accomplish the desired objective. Other solutions are possible. For each of the diodes shown, V_f = 0.7 V.


R
D1
1.3 V
VIN
2.3 V
VOUT
D2
R
D1
VZK = 1.3 V
VIN
VOUT
D2
VZK = 2.3 V