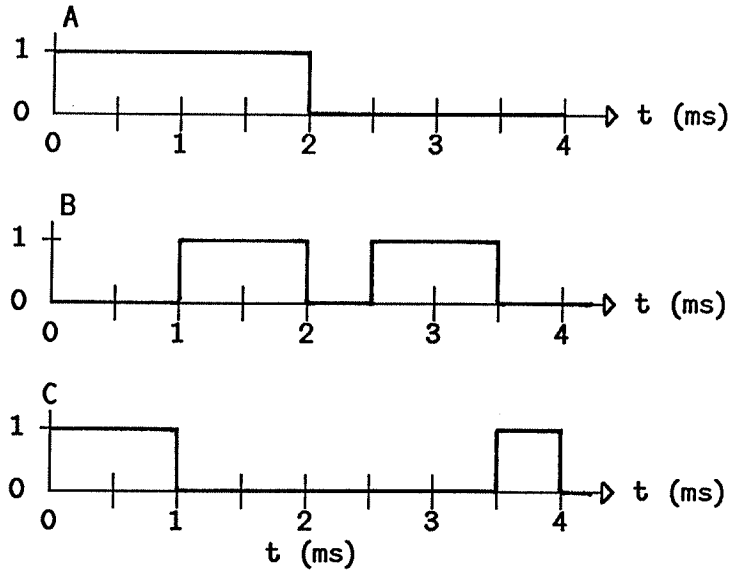
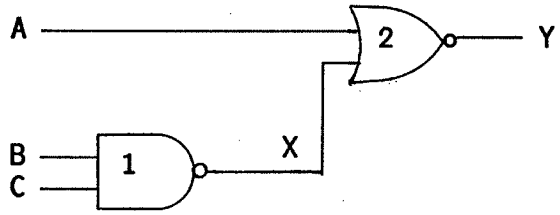
16.1 Three streams of digital data are shown below. Plot Y versus time for the logic function Y = (A*B) + C.

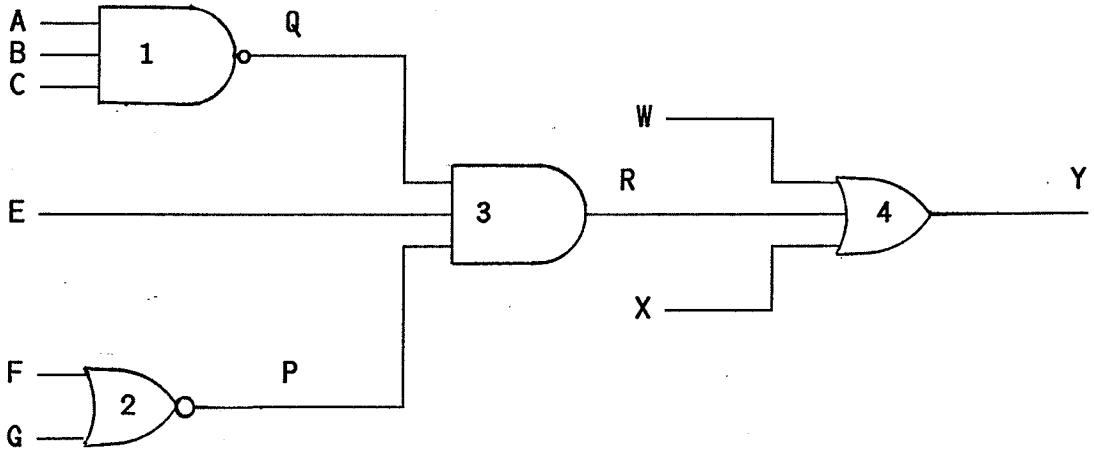


16.2 Repeat Prob. 16.1 for Y = A * (B + C).

16.3 Determine the logic function performed by the following circuit:



16.4 Determine the logic function performed by the following circuit:



16.5 A logic inverter has propagation delays of t_{PHL} = 20 ns and t_{PLH} = 30 ns. One particular logic path involves a series connection through six such gates. What is the overall propagation delay between the input and the output?

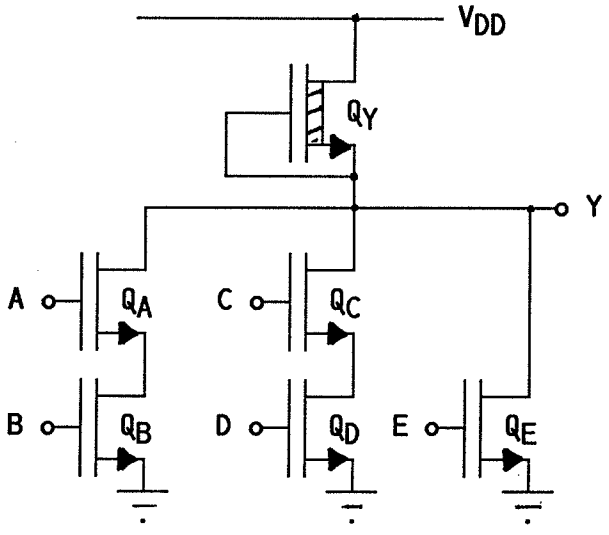
16.6 A logic gate draws 5 mA from a 5-V supply when v_{OUT} is low and 2 mA when v_{OUT} is high. Find the average static power dissipation in the gate for a 50% duty cycle.

16.7 Repeat Prob. 16.6 for a 25% high duty cycle.

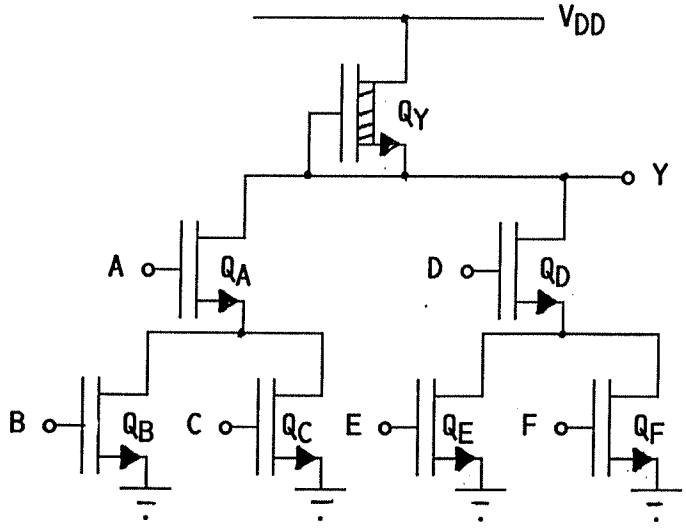
16.8 A logic gate has propagation delay times t_{PHL} = 20 ns and t_{PLH} = 10 ns. As specified in Prob. 16.6, the gate draws 5 mA from a 5-V supply when v_{OUT} is low and 2 mA when v_{OUT} is high. Its output logic levels are V(1) = 4.8 V and V(0) = 0.2 V. Estimate the value of the delay power product for a 50% duty cycle if the gate drives a 10 pF load capacitance and is switched at a 1 MHz rate.

16.9 Consider the logic gate specified in Prob. 16.8. Estimate the value of the delay power product for a 30% high duty cycle if the gate drives a 10 pF load capacitance and is switched at a 5 MHz rate.

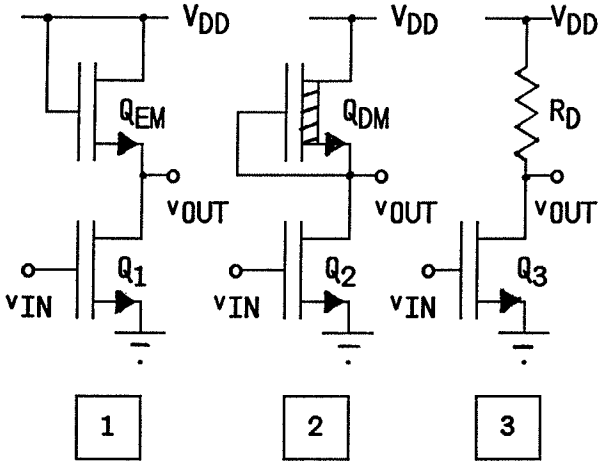
16.10 A digital MOSFET circuit is shown below. To what logic family does this gate belong? Determine the logical function performed by the circuit.



16.11 A digital MOSFET circuit is shown below. To what logic family does this gate belong? Determine the logical function performed by the circuit.



16.12 Three MOSFET inverters are shown below. Which inverter has the lowest value of V_{OH}?



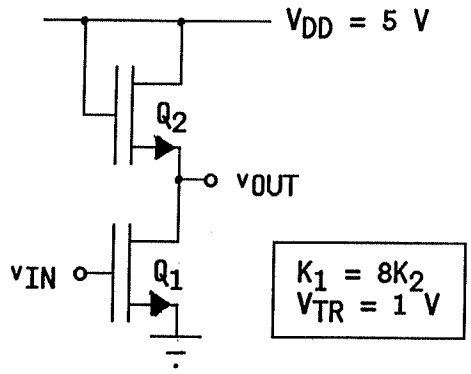
16.13 Consider the three inverters shown above. Which one requires the least amount of time to change from V_{OL} to V_{OH} when a HI-LO step function is applied to v_{IN}?

16.14 The inverters in a particular set of NMOS gates have a relative K-ratio K_R of six. If the smallest device dimension is 1 μm, specify the W and L values of the driving device and pullup load of a single inverter.

16.15 For the NMOS logic family described in Prob. 16.14, estimate the surface area occupied by a single-input inverter.

16.16 For the NMOS logic family described in Prob. 16.14, estimate the surface area occupied by a two-input NOR gate.

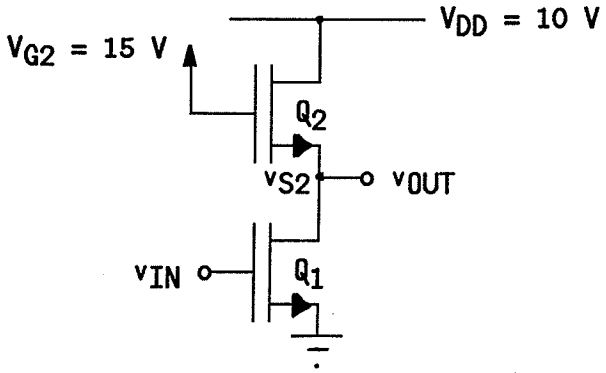
16.17 In the NMOS enhancement-mode inverter shown below, $K_1 = 8K_2$. For both devices, $V_{TR} = 1$ V. When $v_{IN} = 0$, v_{OUT} becomes $V_{DD} - V_{TR}$. Find the value of v_{IN} that will cause v_{OUT} to equal $V_{DD} - 2V_{TR}$, i.e. a voltage drop of V_{TR} below $V_{OH} = V_{TR}$.



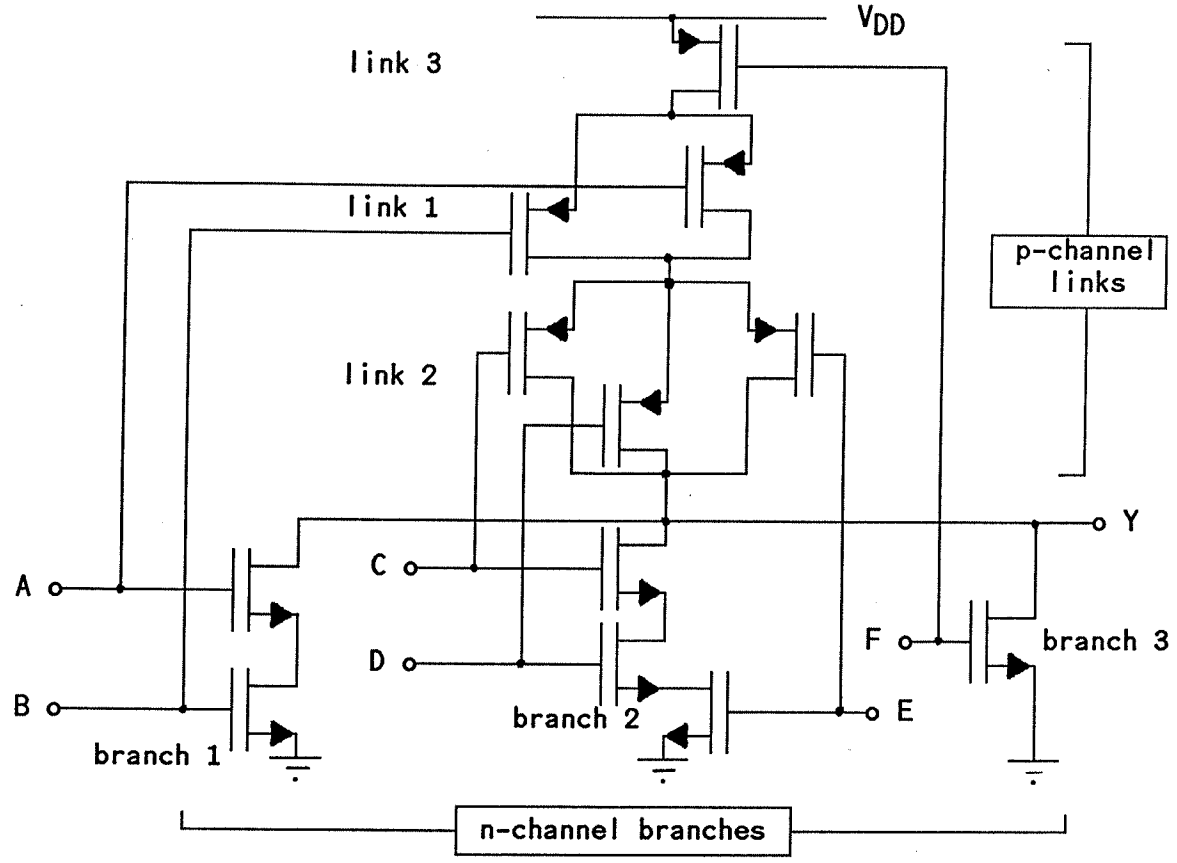
16.18 Consider the enhancement-mode NMOS inverter of Prob. 16.17. Find the value of v_{IN} such that $v_{OUT} = v_{IN}$, i.e., the midpoint of the inverter transfer characteristic.

16.19 Consider the enhancement-mode NMOS inverter of Prob. 16.17. Find the value of v_{IN} such that $v_{OUT} = 1.05V_{TR}$. What condition is associated with this operating point?

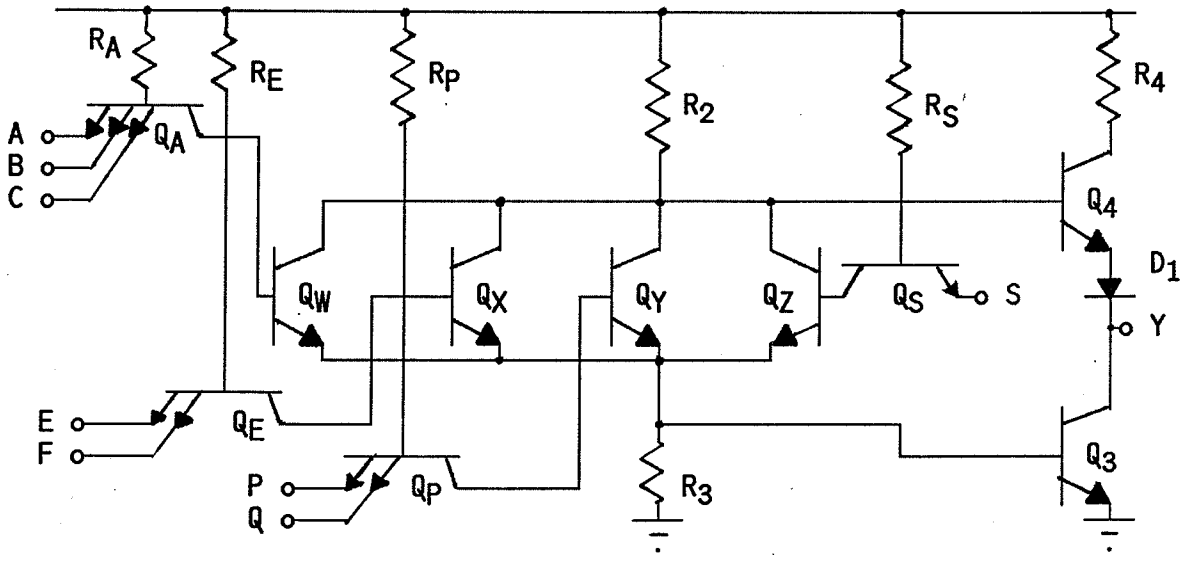
16.20 The NMOS inverter circuit shown below forms one gate in a multi-gate logic circuit. For both devices, $V_{TR} = 2$ V; The W/L ratios are such that $K_1 = 4K_2$. In what region will Q_2 operate? What is the value of v_{OUT} when v_{IN} is low? When v_{IN} is high?



16.21 Consider the MOSFET circuit shown below. To what logic family does this gate belong? What logic function is implemented?



16.22 Consider the BJT circuit shown below. To what logic family does this gate belong? What logic function is implemented?



16.23 A sample-and-hold circuit draws 1 μA from its holding capacitor while in "hold" mode. The circuit is used in an A/D system that samples data every 5 ms. How large must the holding capacitor be if the S/H output is to droop no more that 1 mV while in the hold mode?

16.24 A sample-and-hold circuit has a holding capacitor of 0.5 μF, from which it draws 250 nA while in the "hold" mode. Find the maximum permissible time interval between sample operations if the output is to droop by no more than 0.5 mV during "hold".

16.25 The acquisition time T_a of a sample-and-hold circuit (the time required to charge its holding capacitor) is to be no more than 10 μs. The sampled input will have a maximum magnitude of 10 V, but could be positive or negative. The S/H circuit operates from bipolar power supplies and supplies a constant capacitor charging current. If the holding capacitor is set to 0.005 μF, how much charging current must the S/H circuit be capable of providing?

Performing such an iterative calculation yields the value $V_{CC}/V_{EE} = -1.97 \simeq -2$. One possibility might be $V_{CC} = 16$ V, $V_{EE} = -8$ V.

With the values of V_{CC} and V_{EE} chosen so as to yield a 40%–60% duty cycle, we next must choose R_X and C_X so as to make the total period 1 ms. From Eqn. (15.12):

$$t_1 = R_X C_X \ln \frac{V_{CC} - V_{EE}/2}{V_{CC}/2} = 0.4 \text{ ms}$$

Substituting $V_{CC}/V_{EE} \simeq -2$ results in

$$R_X C_X \ln [2 - (-2)^{-1}] = 0.4 \text{ ms}$$

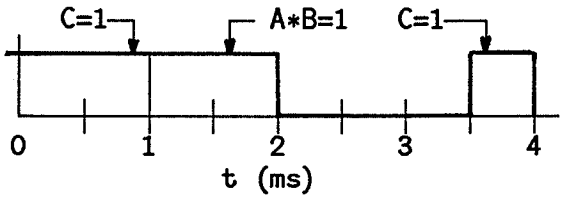
or

$$R_X C_X = \frac{0.4 \text{ ms}}{\ln 2.5} = 0.437 \text{ ms} \simeq 0.44 \text{ ms}$$

The values $C_X = 0.022\ \mu$F; $R_X = 20$ kΩ, for example, will do the job.

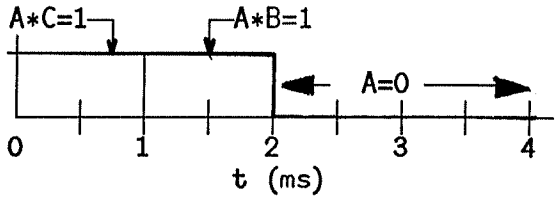
Chapter 16

16.1 The output will be high when C is high or when the product A*B is high (both A and B high). Here is a plot of Y = (A*B) + C:



16.2 The output will be high when A is high and either B or C is high. A plot of the output versus time is shown below. Note that the output can be expressed as

$$Y = A * (B + C) \equiv A*B + A*C.$$



16.3 The output of gate 1 is $X = \overline{B*C}$

The output of gate 2 is

$$Y = \overline{A + X} = \bar{A} * \bar{X} = \bar{A} * \overline{\overline{B*C}} = \bar{A} * B*C$$

16.4 The output of gate 1: $Q = \overline{A*B*C}$

The output of gate 2: $P = \overline{F + G}$

The output of gate 3:

$$R = Q*E*P = \overline{A*B*C} * E * (\overline{F + G})$$

The output of gate 4:

$$Y = W + R + X =$$

$$= W + [(\overline{A*B*C}) * E * (\overline{F + G})] + X$$

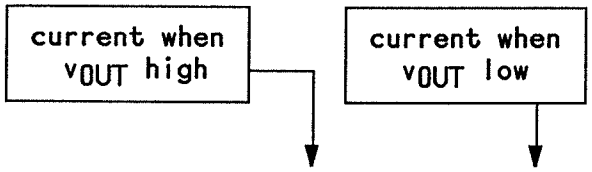
$$= W + [(\bar{A} + \bar{B} + \bar{C}) * E * \bar{F}*\bar{G}\ ] + X$$

16.5 Assume that an inversion function is involved at each gate. For such a system, a low-to-high transition in one gate will always be accompanied by a high-to-low transition in another gate. For six gates, the total delay becomes $3t_{PHL} + 3t_{PLH} = 3(20 \text{ ns} + 30 \text{ ns}) = 150$ ns. Note that this value is equal to six times the average $(t_{PHL} + t_{PLH})/2 = 25$ ns.

16.6 For a 50% duty cycle, the time average static power dissipation will equal the algebraic average of the power drawn by the gate in the high and low states:

$$\langle P_{stat} \rangle = \frac{(5\ V)(5mA + 2mA)}{2} = 17.5\ mW$$

16.7 For an asymmetric duty cycle, the high and low power values must be appropriately weighted when computing the time-average static power:



$$\langle P_{stat} \rangle = [(0.25)(2mA) + (0.75)(5mA)] \times (5\ V) = 21.25\ mW$$

16.8 First compute the energy stored in the load capacitance for high and for low output conditions. Knowledge of these quantities is necessary for an estimate of the time average dynamic power dissipation $\langle P_{dyn} \rangle$. With the output high:

$$E_H = \frac{CV(1)^2}{2} = \frac{(10\ pF)(4.8\ V)^2}{2}$$

$\simeq$ 115.2 pJ. With the output low:

$$E_L = \frac{CV(0)^2}{2} = \frac{(10\ pF)(0.2\ V)^2}{2} \simeq 0.2\ pJ$$

When the load capacitance is charged from V(0) to V(1), an amount of energy equal to $E_H - E_L$ must be provided by the power supply. This energy increment is stored in the load capacitance. As discussed in the text, the supply must also provide an additional amount of energy equal to $E_H - E_L$ for dissipation in the components of the gate during the charging process.

When C_L is discharged from V(1) to V(0), the energy stored during charging will be lost (dissipated in the gate or other load components). The energy quantity $E_H - E_L$ must be replenished the next time the capacitor is charged, requiring that an equal amount again be dissipated in the gate. Thus each complete cycle of capacitor charge and discharge requires that $2(E_H - E_L) = 2(115.2\ pJ - 0.2\ pJ) = 230\ pJ$ be provided by the power supply.

At a 1 MHz rate, the gate is switched through a complete low-to-high-to-low cycle on the order of once every 1 μs, hence the time-average dynamic power $\langle P_{dyn} \rangle$ becomes

$$\frac{2(E_H - E_L)}{T} = \frac{230\ pJ}{1\ \mu s} = 0.23\ mW$$

Next compute the time-average static power dissipation $\langle P_{stat} \rangle$. For a 50% duty cycle, the time-average static power $\langle P_{stat} \rangle$ is

$$\frac{5\ V(5\ mA + 2\ mA)}{2} = 17.5\ mW,$$

as shown in Prob 16.6. The total time-average dissipated power thus becomes $\langle P_d \rangle = \langle P_{stat} \rangle + \langle P_{dyn} \rangle = 17.5\ mW + 0.23\ mW = 17.7\ mW$. Note that $\langle P_{stat} \rangle$ constitutes the major source of energy loss in the gate.

Finally, compute the delay-power product of the gate. For the average time delay

$$t_D = \frac{t_{PHL} + t_{PLH}}{2} = \frac{20\ ns + 10\ ns}{2}$$

= 15 ns, the delay-power product becomes $t_D\langle P_d \rangle = (15\ nS)(17.7\ mW) \simeq 266\ pJ$.

16.9 For the 10 pF load of Prob. 16.8, the changes in duty cycle and cycling time do not change E_H or E_L. Hence the energy lost during each charge-discharge cycle is again $2(E_H - E_L) = 2(115.2\ \text{pJ} - 0.2\ \text{pJ}) = 230\ \text{pJ}$. At a 5 MHz rate, the cycle time becomes 0.2 μs, so that $\langle P_{dyn} \rangle = \dfrac{2(E_H - E_L)}{T} = \dfrac{230\ \text{pJ}}{0.2\ \mu\text{s}} = 1.15\ \text{mW}$

For a 30% high duty cycle, the time-average static power becomes

$$\langle P_{stat} \rangle = [(0.3)(2\ \text{mA}) + (0.7)(5\ \text{mA})] \times (5\ \text{V}) = 20.5\ \text{mW}$$

The total time-average dissipated power thus becomes $\langle P_d \rangle = \langle P_{stat} \rangle + \langle P_{dyn} \rangle = 20.5\ \text{mW} + 1.15\ \text{mW} \simeq 21.7\ \text{mW}$. Note that $\langle P_{stat} \rangle$ still constitutes the major source of energy loss in the gate, even though $\langle P_{dyn} \rangle$ is five times larger at the faster switching rate. The value of t_D remains the same for this problem, so that the delay-power product becomes

$$t_D \langle P_d \rangle = (15\ \text{nS})(21.7\text{mW}) \simeq 325\ \text{pJ}.$$

16.10 This circuit is a multi-input NMOS logic gate (enhancement-mode input devices; depletion-mode pullup load). The left-hand leg will force Y low when both A and B are high. The middle leg will force Y low when both C and D are high. The right-hand leg will force Y low when E is high. The three legs are connected in parallel (OR function), hence the output becomes

$$Y = \overline{A*B + C*D + E}$$

16.11 This circuit is a multi-input NMOS logic gate (enhancement-mode input devices; depletion-mode pullup load). The lower-left collection of devices will force Y low for A high and B or C high. Similarly, the lower-right collection of devices will force Y low for D high and E or F high. These branches are connected in parallel (OR function), hence the output becomes

$$Y = \overline{A*(B + C) + D*(E + F)}$$

16.12 Inverter #1 has the lowest V_{OH}. For inverter #1, $v_{OUT} = V_{DD} - V_{TR}$ when v_{IN} is low (Q_1 in cutoff). For the other two inverters, v_{OUT} is equal to V_{DD} when v_{IN} is low.

16.13 The transition time of v_{OUT} will be determined by the net load capacitance C_L and by the current available to charge it. The former consists of the C_{GS} of any gates driven by v_{OUT} plus any internal capacitance components contributed by the gate's own MOSFETs. For equal load capacitances, inverter #2 will have the shortest transition time, since it will provide the largest overall charging current. Specifically, when v_{OUT} begins to increase, the current through Q_2 will remain constant for most of the transition, leading to the largest $dv_{OUT}/dt = i_D/C_L$. In the other inverters, the current available to charge C_L is determined by the voltage across the pullup load (i.e., Q_{EM} or R_D). The charging current will thus decrease as v_{OUT} increases.

16.14 Call the driven device Q_1 and the pullup load Q_2. The problem specifies that $K_R = K_1/K_2 = 6$. The K parameter for a MOSFET is proportional to W/L, hence this constraint becomes

$$K_R = \frac{K_1}{K_2} = \frac{W_1}{L_1}\frac{L_2}{W_2} = 6$$

Note that all the other factors contained in K_1 and K_2 cancel out of this equation. If the smallest device dimension is 1 μm, the above condition on K_R can be satisfied by the values

$$W_1 = 6\ \mu m$$
$$L_1 = L_2 = W_2 = 1\ \mu m$$

Another alternative might be

$$W_1 = L_2 = \sqrt{6} \simeq 2.5\ \mu m$$
$$L_1 = W_2 = 1\ \mu m$$

16.15 For the answer given in Prob. 16.14, the area of the driving device Q_1 is

$$W_1L_1 = 6\ \mu m \times 1\ \mu m = 6\ \mu m^2$$

The area of the pullup load Q_2 is

$$W_2L_2 = 1\ \mu m \times 1\ \mu m = 1\ \mu m^2$$

The total area becomes

$$W_1L_1 + W_2L_2 = 6\ \mu m^2 + 1\ \mu m^2 = 7\ \mu m^2$$

These calculations assume that the gate surface represents the major portion of area occupied by the devices. The actual chip area would be slightly larger since the drain, source, and perimeter regions of each device would require a small amount of additional area.

For the second solution given,

$$W_1L_1 = \sqrt{6}\ \mu m \times 1\ \mu m = \sqrt{6}\ \mu m^2$$
$$W_2L_2 = 1\ \mu m \times \sqrt{6}\ \mu m = \sqrt{6}\ \mu m^2$$

The total inverter area becomes

$$W_1L_1 + W_2L_2 = 2\sqrt{6}\ \mu m^2 = 4.9\ \mu m^2$$

Note that the second solution results in a smaller overall surface area.

16.16 In an NMOS NOR gate, any one input device can be used to force the output low. Each parallel input must thus have the W and L values required for a single input inverter. A K_R of six can be realized with the device dimensions found in Prob. 16.14. A two-input NOR gate will thus have a total area of

$$W_{1A}L_{1A} + W_{1B}L_{1B} + W_2L_2 =$$
$$6\ \mu m^2 + 6\ \mu m^2 + 1\ \mu m^2 = 13\ \mu m^2$$

The alternative solution yields

$$W_{1A}L_{1A} + W_{1B}L_{1B} + W_2L_2 =$$
$$\sqrt{6}\ \mu m^2 + \sqrt{6}\ \mu m^2 + \sqrt{6}\ \mu m^2 \simeq 7.3\ \mu m^2$$

The second solution clearly results in a much smaller total gate area.

16.17 The devices share the same current, and Q_2 automatically operates in the constant-current region (gate connected to drain). Assume Q_1 to also operate in the constant-current region and equate their current expressions:

$$K_1(v_{GS1} - V_{TR})^2 = K_2(v_{GS2} - V_{TR})^2$$
$$K_1(v_{IN} - V_{TR})^2 = K_2(V_{DD} - v_{OUT} - V_{TR})^2$$

For the condition

$$v_{OUT} = V_{DD} - 2V_{TR},$$

the above equation becomes

$$K_1(v_{IN} - V_{TR})^2 = K_2V_{TR}^2$$

or

$$v_{IN} = \left[\sqrt{\frac{K_2}{K_1}} + 1\right]V_{TR} = \left[\sqrt{\frac{1}{8}} + 1\right](1\ V)$$
$$= 1.35\ V$$

Note that Q_1 indeed operates in the constant-current region for this v_{IN}:

$$v_{DS1} > v_{GS1} - V_{TR}$$

$$v_{OUT} > v_{IN} - V_{TR}$$

$$3\ V > 1.35\ V - 1\ V = 0.35\ V$$

where $v_{OUT} = V_{DD} - 2V_{TR} = 3\ V$.

16.18 The current through both devices must be the same. With gate connected to drain, Q_2 automatically operates in the constant-current region. When $v_{OUT} = v_{IN}$, Q_1 will also operate in the constant-current region, e.g. the condition

$$v_{DS1} > v_{GS1} - V_{TR},$$

which implies the condition

$$v_{OUT} > v_{IN} - V_{TR},$$

will be met for $v_{OUT} = v_{IN}$ and V_{TR} positive:

$$v_{IN} > v_{IN} - V_{TR}.$$

Equating the expressions for drain current with $v_{OUT} = v_{IN}$ results in

$$K_1(v_{IN} - V_{TR})^2 = K_2(V_{DD} - v_{IN} - V_{TR})^2$$

Solving for v_{IN} yields

$$v_{IN} = \left[\frac{K_2}{K_1}\right]^{1/2}(V_{DD} - v_{IN} - V_{TR}) + V_{TR}$$

or

$$v_{IN} = \frac{\left[\frac{K_2}{K_1}\right]^{1/2}(V_{DD} - V_{TR}) + V_{TR}}{1 + (K_2/K_1)^{1/2}}$$

In this case, $(K_2/K_1)^{1/2} = \sqrt{1/8} = 0.35$, so the above becomes

$$v_{IN} = \frac{0.35\ (5\ V - 1\ V) + 1\ V}{1 + 0.35} = 1.78\ V$$

16.19 See solution to Prob. 16.18.

For $v_{OUT} = 1.05V_{TR} = 1.05$ V, the equation for v_{IN} becomes

$$v_{IN} = \left[\frac{K_2}{K_1}\right]^{1/2}(V_{DD} - v_{OUT} - V_{TR}) + V_{TR}$$

$$= \left[\frac{K_2}{K_1}\right]^{1/2}(V_{DD} - 2.05V_{TR}) + V_{TR}$$

$$= \sqrt{\frac{1}{8}}(5\ V - 2.05\ V) + 1\ V = 2.04\ V$$

The constant-current region condition

$$v_{DS1} > v_{GS1} - V_{TR}$$

i.e.

$$1.05\ V > 2.04\ V - 1\ V = 1.04\ V$$

is just barely met for this value of v_{OUT}. The computed operating point represents the entry of Q_1 into the triode region.

16.20 The gate of Q_2 is set to 15 V and its drain to 10 V. Test for constant-current region operation:

$$v_{DS2} > v_{GS2} - V_{TR} \quad (?)$$

$$V_{DD} - v_{S2} > V_{G2} - v_{S2} - V_{TR} \quad (?)$$

$$10\ V - v_{OUT} > 15\ V - v_{OUT} - 2\ V \quad (?)$$

$$10\ V > 13\ V \quad (?)$$

The test fails, hence Q_2 is forced to operate in the triode region.

When v_{IN} is low, Q_1 will be in cutoff. The current through Q_2 will also be zero, so that $v_{DS2} = 0$ and $v_{OUT} = V_{DD} = 10$ V. Under these conditions, $v_{GS2} = 15\ V - 10\ V = 5$ V.

When v_{IN} is high (i.e., equal to V_{DD} from some other gate), Q_1 will conduct. The gate of Q_1 will be held at 10 V and its drain at a much lower voltage. These conditions are conducive to triode-region operation, hence Q_1 can be assumed to operate in the triode region; this assumption must be confirmed later. The current through each device is the same, hence, for triode region operation in both devices, $K_2[2(v_{GS2} - V_{TR})v_{DS2} - (v_{DS2})^2]$

$$= K_1[2(v_{GS1} - V_{TR})v_{DS1} - (v_{DS1})^2]$$

In this case, $v_{GS2} = V_{G2} - v_{OUT}$, $v_{DS2} = V_{DD} - v_{OUT}$, $v_{GS1} = v_{IN}$, and $v_{DS1} = v_{OUT}$. Substituting these voltages into the triode region current equations results in

$$2(V_{G2} - v_{OUT} - V_{TR})(V_{DD} - v_{OUT}) - (V_{DD} - v_{OUT})^2 = (K_1/K_2)[2(v_{IN} - V_{TR})v_{OUT} - (v_{OUT})^2]$$

Substituting numerical voltage values, with $v_{IN} = 10$ V, $V_{TR} = 1$ V, and $K_1/K_2 = 4$, results in

$$2(14\text{ V} - v_{OUT})(10\text{ V} - v_{OUT}) - (10\text{ V} - v_{OUT})^2 = 4\,[2(9\text{ V})v_{OUT} - (v_{OUT})^2]$$

Algebraic reduction results in

$$(v_{OUT})^2 - (20\text{ V})v_{OUT} + (36\text{ V}^2) = 0$$

This quadratic equation has solutions

$$v_{OUT} = \frac{20\text{ V} \pm \sqrt{(20\text{ V})^2 - 4(36\text{ V}^2)}}{2}$$

$$= 2\text{ V},\ 18\text{ V}$$

The second value represents a mathematical, but not electronic solution, because it is larger than the available V_{DD}; hence $v_{OUT} = 2$ V.

For this value of v_{OUT}, Q_1 is confirmed to operate in the triode region:

$v_{DS1} < v_{GS1} - V_{TR}$ (?)
$v_{OUT} < v_{IN} - 1\text{ V}$ (?)
$2\text{ V} < 10\text{ V} - 1\text{ V} = 9\text{ V}$ (?)

Triode region operation is confirmed.

16.21 This circuit forms a multi-input CMOS logic gate. The n-channel devices form three possible branches between Y and ground. If any one of these parallel n-channel branches is made conducting, the output Y will be low. A given n-channel branch will be broken if any one of its inputs is low. If such a condition occurs, the branch's companion p-channel link will be made conducting, helping to connect Y to V_{DD}. If all the n-channel branches are broken, all the p-channel links will made conducting, and Y will be connected to V_{DD}. Thus the output Y will be zero for any of the following conditions:

A and B high (branch 1)
C and D and E high (branch 2)
F high (branch 3)

i.e. $Y = \overline{A*B + C*D*E + F}$

16.22 This circuit forms a multi-input TTL logic gate. If any of the parallel transistors Q_W, Q_X, Q_Y, or Q_Z conducts, Q_4 will go into cutoff and the output will be low. Any one of these parallel transistors will conduct if all of the emitter leads of its input transistor are held high; e.g. Q_W will conduct if A = B = C = 1. Thus Y = 0 for any of the following conditions.

A and B and C high (Q_A)
E and F high (Q_E)
P and Q high (Q_P)
S high (Q_S)

i.e. $Y = \overline{A*B*C + E*F + P*Q + S}$

16.23 The capacitor must be large enough so that it will not discharge toward zero by more than 1 mV while the S/H is in the "hold" mode. The capacitor is charged to the sampled voltage during the "sample" operation. In this case, the current drawn from the capacitor during "hold" is constant, hence the capacitor will discharge at a constant rate, drooping a total of

$$\Delta v_C = \frac{dv_C}{dt} T = \frac{I_C}{C} T$$

where T is the time between sample operations and $I_C = -1\ \mu A$ for positive v_C. If the capacitor voltage is to decay by no more than -1 mV between sample operations, C must exceed the value

$$\frac{I_C}{\Delta v_C} T = \frac{-1\ \mu A}{-1\ mV} (5\ ms) = 5\ \mu F$$

16.24 The current drawn on the holding capacitor is constant, hence the capacitor voltage will decay at a constant rate $dv_C/dt = I_C/C$. (For a positive v_C, I_C is negative out of the capacitor). If Δv_C is not to exceed -0.5 mV, the maximum time interval between sample operations must not exceed

$$T = \frac{C\Delta v_C}{I_C} = \frac{(0.5\ \mu F)(0.5\ mV)}{250\ nA} = 1\ ms$$

16.25 Assume worst case conditions, i.e., the capacitor must be charged all the way from -10 V to 10 V ==> $\Delta v_C = 20$ V. Given that $dv_C/dt = I_C/C$ for a constant capacitor charging current, the required minimum I_C for charging in $T_a = 10\ \mu s$ becomes

$$I_C = \frac{C\Delta v_C}{T_a} = \frac{(0.005\ \mu F)(20\ V)}{10\ \mu s} = 10\ mA$$
