MOSFET DIFFERENTIAL AMPLIFIER (TWO-WEEK LAB)

BACKGROUND

The MOSFET is by far the most widely used transistor in both digital and analog circuits, and it is the backbone of modern electronics. One of the most common uses of the MOSFET in analog circuits is the construction of differential amplifiers. The latter are used as input stages in op-amps, video amplifiers, high-speed comparators, and many other analog-based circuits. MOSFET differential amplifiers are used in integrated circuits, such as operational amplifiers, they provide a high input impedance for the input terminals. A properly designed differential amplifier with its current-mirror biasing stages is made from matched-pair devices to minimize imbalances from one side of the differential amplifier to the other.

In this lab, you will design a differential amplifier by first verifying its operation in PSPICE, then building and testing your circuit stage by stage.

In your lab kit, you will find one or more CD4007 integrated circuits. (The letter prefix may vary; it's the number 4007 that matters.) This IC contains a number of NMOS and PMOS devices, as shown below. You may assume that all the NMOS transistors are matched to each other (same value of $K$ and threshold voltage $V_{TH}$), and that all the PMOS devices are similarly matched to each other. Use the devices in this integrated circuit when building your differential amplifier, as requested in Levels 2 and 3.
BACKGROUND

The general topology of a differential amplifier is shown below. Two active devices are connected to a positive voltage supply via passive series elements. The transistors must be a matched pair (i.e., two matched MOSFETs or two matched BJTs). The "pull up" loads are similarly matched to each other. The lower terminals of the active devices are connected together, and a dc current source pulls current down toward the negative voltage bus to effect the bias. The controlling input ports of the devices are connected to input signals.

If the input signals are designated $v_1$ and $v_2$, they can be decomposed into two linear combinations, one called the differential mode, and the other the common mode. The differential mode is defined by the following equation:

$$v_{idm} = v_1 - v_2$$

Similarly, the common mode, equal to the average value of the signals, is defined by:

$$v_{icm} = \frac{v_1 + v_2}{2}$$

These definitions allow the actual input signals $v_1$ and $v_2$ to be expressed as linear combinations of their differential and common modes:

$$v_1 = v_{icm} + \frac{v_{idm}}{2} = \frac{v_1 + v_2}{2} + \frac{v_1 - v_2}{2} = v_1$$

$$v_2 = v_{icm} - \frac{v_{idm}}{2} = \frac{v_1 + v_2}{2} - \frac{v_1 - v_2}{2} = v_2$$

because the small-signal model of the amplifier is linear, its total response will be equal to the superposition of its responses to, respectively, the differential and common modes of the input signals.
**Current Mirror.**
The common-mode gain of the differential amplifier will be small (desirable) if the small-signal Norton, resistance $r_n$ of the biasing current source is large. As we have discussed in class, the biasing current source is not a naturally occurring element, but must be synthesized from other transistors. In most situations, the designer will choose some form of *current mirror* to produce the equivalent current source. The circuit on the left, shown below, is equivalent in all respects to the symbolic current-source component on the right.

In the current mirror circuit shown on the left, the reference current is set by the resistor. The voltage across the latter is given by the voltage drop across $R_{\text{ref}}$. Because the two MOSFETs are matched, and have precisely the same gate-source and threshold voltages ($v_{\text{GSA}} = v_{\text{GSB}}$), their drain currents will be equal. Thus, the current $I_o$ becomes a replica, or "mirror image" of the reference current. As long as $Q_B$ remains in its constant current region, then this replication will take place. Note that $Q_A$ automatically operates in its constant current region, because it's gate is connected to its drain.

The Norton resistance $r_n$ the current source will be equal to the output resistance $r_o$ of $Q_B$, as determined by the upward slope of that transistor's voltage-current characteristic. The latter is associated with the Early voltage, as discussed in class and in the text.

**MOSFET Conductance Parameter.**

If one studies the semiconductor physics that makes a MOSFET work, one can determine that the following formula gives the value of conductance parameter $K$:

$$K = (\mu e \epsilon_{\text{ox}} / 2 \epsilon_{\text{ox}})(W/L)$$
The constant $\mu_e$ is the electron mobility of the semiconductor, and $\varepsilon_{\text{ox}}$ is the dielectric constant of the oxide layer under the MOSFET gate. The parameter $t_{\text{ox}}$ is the physical thickness of the gate oxide layer.

Two key parameters are the width $W$ and length $L$ of the MOSFET as it is laid out on the integrated circuit. $L$ is the distance between the drain and source terminals, and $W$ is the lateral width of the entire device, as shown below:

![Diagram showing the physical dimensions of a MOSFET](image)

**Level 1:**
Consider the circuit shown below, for which the following parameters may be assumed: $|V_{\text{TR}}| = 1 \text{ V}$, $K_N = 2 \times 10^{-5} \text{ A/V}^2$, $K_P = 10^{-5} \text{ A/V}^2$ and $V_A = 100 \text{ V}$ (that is, the channel-width parameter $\lambda = 0.01 \text{ V}^{-1}$). Here, the conductance parameters $K_N$ and $K_P$ are the values that a device of dimension 1 $\mu$m $\times$ 1 $\mu$m device would have (i.e., $W = L = 1 \mu$m).

The fractional number next to each MOSFET symbol shows its $W/L$ ratio (length and width values given in microns).

![Circuit diagram](image)

$V_{\text{TRN}} = |V_{\text{TRP}}| = 1 \text{ V}$. $\mu_e C_{\text{ox}} = 20 \mu\text{A/V}^2$, $\mu_h C_{\text{ox}} = 10 \mu\text{A/V}^2$, and $V_{\text{AN}} = V_{\text{AP}} = 100 \text{ V}$. 
a) Use PSPICE to find the bias values of all the numbered node voltages. Record them in your notebook, then compare them with the values computed by hand, and provided in the Appendix.

b) Use PSPICE to plot the output voltage at nodes 2, 3, and $v_{out}$ in response to a differential-mode input. Specifically, sweep $v_1$ from $-1\text{mV}$ to $+1\text{mV}$, and make $E_2$ equal to $-v_1$.

**Level 2**

Build the current mirror circuit shown to the right. Use two of the NMOS devices on your 4007 chip. Your current mirror will pull current out of an external circuit comprised of a 10-kΩ resistor and an 8-V dc source.

Measure $I_{D3}$ with either an ammeter, or by measuring the voltage drop across $R_1$ and applying Ohm's law. Confirm that $I_{D4}$ is the mirror image of $I_{D3}$; that is $I_{D4} = I_{D3}$.

**Level 3**

Using the current mirror from Level 2, use additional transistors to build the differential amplifier shown to the right.

a) Confirm that the bias values $V_{D1}$ and $V_{D2}$ to lie approximately midway between the two supply voltages $V_{DD}$ and $V_{SS}$.

b) Measure and record the differential-mode and common-mode gains of your amplifier.
APPENDIX

- **Find the bias currents through each leg of the current mirror**
  Given that \( I_A = I_o = 20 \ \mu A \), the various bias currents become, via Eqs. (12.67) and (12.68),
  \[
  I_B = \frac{W_B/L_B}{W_A/L_A} I_o = \frac{20/100}{10/10} 20 \ \mu A = 4 \ \mu A
  \]
  \( (12.76) \)
  and
  \[
  I_C = \frac{W_C/L_C}{W_A/L_A} I_o = \frac{10/10}{10/10} 20 \ \mu A = 20 \ \mu A
  \]
  \( (12.77) \)

- **Find the bias value of node voltage \( V_C \)**
  This node voltage will be equal to \( V_{DD} - V_{SG3} \). Computing the gate-to-source voltage \( V_{SG3} = -V_{GS3} \) requires knowledge of \( |K_3| \). From the given data,
  \[
  |K_3| = \frac{1}{2} \frac{W_3}{L_3} \mu \alpha C_{ox} = \frac{5}{2(11)} (10 \ \mu A/V^2) = 2.27 \ \mu A/V^2
  \]
  \( (12.78) \)
  Using this value of \( |K_3| \), and the value \( I_3 = I_B/2 = 2 \ \mu A \), it follows that
  \[
  V_{SG3} = (I_3/|K_3|)^{1/2} + |V_{TRP}|
  = [(2 \ \mu A)/(2.27 \ \mu A/V^2)]^{1/2} + 1 \ V \approx 1.9 \ V
  \]
  \( (12.79) \)
  and
  \[
  V_C = V_{DD} - V_{SG3} = 5 \ V - 1.9 \ V = 3.1 \ V
  \]

- **Find the bias value of node voltage \( V_B \)**
  For the \( W/L \) values indicated in Table 1, the \( K \) parameters of \( Q_1 \) and \( Q_2 \) become
  \[
  K_1 = K_2 = \frac{1}{2} \frac{W_1}{L_1} \mu \alpha C_{ox} = \frac{20}{2(5)} (20 \ \mu A/V^2) = 40 \ \mu A/V^2
  \]
  \( (12.80) \)
  With \( I_1 = I_2 = I_B/2 = 2 \ \mu A \), and with \( v_1 \) and \( v_2 \) held at dc ground by input signal sources, it follows that
  \[
  V_{GS1} = V_{GS2} = (I_1/K_1)^{1/2} + V_{TRN}
  = [(2 \ \mu A)/(40 \ \mu A/V^2)]^{1/2} + 1 \ V \approx 1.2 \ V
  \]
  \( (12.81) \)
  where \( V_B = 0 - V_{GS1} = -1.2 \ V \).

- **Find the bias value of node voltage \( V_{D2} \)**
  The value of this node voltage is determined by \( V_{SG5} \), which is, in turn, determined by the current
  \[
  I_5 = I_C = \frac{W_C/L_C}{W_A/L_A} I_o = \frac{10/10}{10/10} (20 \ \mu A) = 20 \ \mu A
  \]
  \( (12.82) \)
  and the conductance parameter
  \[
  |K_5| = \frac{1}{2} \frac{W_5}{L_5} \mu \alpha C_{ox} = \frac{90}{2(20)} (10 \ \mu A/V^2) = 22.5 \ \mu A/V^2
  \]
  \( (12.83) \)
  Specifically, from the \( v-i \) equation of \( Q_5 \), it follows that
  \[
  V_{SG5} = (I_5/|K_5|)^{1/2} + |V_{TRP}|
  = [(20 \ \mu A)/(22.5 \ \mu A/V^2)]^{1/2} + 1 \ V \approx 1.9 \ V
  \]
  \( (12.84) \)
  Note that this voltage is identical to \( V_{SG3} \), as computed in Eq. (12.79), because the \( W/L \) ratios of \( Q_B, Q_C, Q_3, \) and \( Q_5 \) satisfy Eq. (12.72). Finally, from KVL,
  \[
  V_{D2} = V_{DD} - V_{SG5} = 5 \ V - 1.9 \ V = 3.1 \ V
  \]
  \( (12.85) \)
  which is identical to the previously computed voltage of node \( C \).
Small Signal Differential-Mode Performance

The CMOS amplifier of Fig. 12.15 will respond to both differential- and common-mode signals. Its gain under differential-mode excitation can be easily derived using the results of Section 8.4.3. In this case, the incremental output resistance \( r_{o4} \) of \( Q_4 \) acts as the pull-up load to \( Q_2 \). As noted in Eq. (8.187), the differential-mode gain observed at the drain of \( Q_2 \), as enhanced by the current-mirror action of \( Q_3 \) and \( Q_4 \), becomes

\[
A_{dm-dc} = \frac{v_{d2}}{v_{dm}} = g_{m2}(r_{o2}||r_{o4})
\]

(12.86)

where \( v_{dm} = v_1 - v_2 \). Because \( r_{o4} \) is comparable to \( r_{o2} \), both resistances are included in the equation.

The signal \( v_{d2} \) from the drain of \( Q_2 \) is fed to the gate of \( Q_5 \). This latter transistor acts as a p-channel inverter actively loaded by \( r_{oc} \) of \( Q_C \). The gain of the second stage thus becomes

\[
\frac{v_{out}}{v_{d2}} = -g_{m5}(r_{oc}||r_{o5})
\]

(12.87)

Note that \( r_{o5} \) is included in this equation because it is comparable to \( r_{oc} \).

The loading of the \( v_{d2} \) node by the gate of \( Q_5 \) is negligible, because the latter presents a pure capacitive load to the former. The overall signal gain of the two-stage cascade thus can be determined by simply multiplying together the individual gain equations (12.86) and (12.87), yielding

\[
A_{dm} = \frac{v_{out}}{v_{dm}} = -g_{m2}g_{m5}(r_{o2}||r_{o4})(r_{oc}||r_{o5})
\]

(12.88)

We note that \( g_m = 2\sqrt{K_D} \) for a MOSFET in the constant-current region, and that \( r_n = V_A/I_D \), where \( V_A \) is the MOSFET's Early voltage. Given that \( I_2 = I_4 \) and \( I_3 = I_5 \), Eq. (12.88) can be expressed in the alternative form

\[
A_{dm} = -(2\sqrt{K_2}I_2)(2\sqrt{K_5}I_5) \frac{V_{d2}}{I_2} \frac{V_{A4}}{I_4} \frac{V_{AC}}{I_C} \frac{V_{A5}}{I_5}
\]

\[
= -4\sqrt{K_2K_5}I_2I_5 \left( \frac{V_{AN}/I_2}{V_{AN}/I_2 + V_{AP}/I_2} \right) \left( \frac{V_{AN}/I_2}{V_{AN}/I_2 + V_{AP}/I_2} \right)
\]

\[
= -4 \left( \frac{K_2K_5}{I_2I_5} \right)^{1/2} \left( \frac{V_{AN}V_{AP}}{V_{AN} + V_{AP}} \right)^2
\]

(12.89)

where \( V_{AN} \) and \( V_{AP} \) are the Early voltages of the n-channel and p-channel devices, respectively. If \( V_{AN} = V_{AP} = V_A \), the last term in Eq. (12.89) becomes \((V_A^2/2V_A)^2 = V_A^2/4\), so that the equation reduces to

\[
A_{dm} = -V_A^2 \left( \frac{K_2K_5}{I_2I_5} \right)^{1/2}
\]

(12.90)

Note that \( A_{dm} \) becomes larger as \( I_2 \) and \( I_5 \) are reduced. This effect occurs because the incremental output resistances \( r_{o2} \), \( r_{o4} \), \( r_{oc} \), and \( r_{o5} \) of \( Q_2 \), \( Q_4 \), \( Q_C \), and \( Q_5 \) become larger with decreasing magnitude of drain current \( I_D \).

As these results show, the circuit designer has several degrees of freedom in setting the gain of a CMOS op-amp. Given knowledge of the process-dependent parameters \( V_T \), \( V_A \), and \( \mu \varepsilon_0/\varepsilon_0 = \mu C_{ox} \) for n-channel and p-channel devices, where \( K = \mu C_{ox}W/(2L) \), the open-loop gain of the amplifier can be set by appropriately choosing the \( W/L \) ratios of each device.