

EC551 - Advanced Digital Design with Verilog and FPGAs Fall 2016

Class: Tuesday and Thursday, 4-6 pm in KCB 106
Lab: Monday & Friday 5-7 pm, Wednesday 12-2pm in PHO 115
Number of Credits: 4
Prerequisites: EC311, EC413 (Recommended)

Course Objectives

Content includes the use of a hardware description language (HDL; in particular Verilog) for the specification, synthesis, simulation, and exploration of principles of register transfer level (RTL) designs. Programmable logic, such as field programmable gate array (FPGA) devices, has become a major component of digital design. In this class the students learn how to write HDL models that can be automatically synthesized into integrated circuits using FPGAs. Laboratory and homework exercises include writing HDL models of combinational and sequential circuits, synthesizing models, performing simulation, writing testbench modules, and synthesizing designs to an FPGA by using automatic place and route EDA tools.

The course material is broken down into three areas: Electronic Design Automation (EDA), Verilog, Reconfigurable Computing (RC), and the course Project. The topics are scheduled and organized so that these topics are woven together in lecture to provide breadth and depth in select areas. Homework (HW) and Lab exercises are created to reinforce lecture material and provide the required knowledge for the larger course project. At the conclusion of the course, the students should understand a digital EDA design flow and how to program reconfigurable computing hardware using this flow.

The course project plays a major role in the course. Students are expected to create a fully demonstrable digital system on an FPGA. This project is done in groups of 4-5 students and should represent 15 hours of work (or more) per student per week.

Staff Information

Instructor

Name: **Prof. Wenchao Li**
Office: PHO 336
Office phone number: 617-353-0115
E-mail address: wenchao@bu.edu (**Best way to contact me - Include "EC551 F16:" in the subject line**)
Office Hours: PHO 336, Tuesdays 2pm-3pm, Thursdays 2pm-3pm or by appointment

Lab Assistants

Name: Kiran Vishal Thanjavur Bhaaskar, Archana Bajaj
E-mail address: vishal94@bu.edu, bajaj@bu.edu (**Include "EC551 F16:" in the subject line**)
Office Hours: by appointment

Course Resources

Required Textbooks

1. Author: M.D. Ciletti
Title: Advanced Digital Design with the Verilog HDL (2nd Edition)
ISBN: 0136019285

Optional Textbooks

1. Author: David R. Smith, Paul Franzon
Title: Verilog Styles for Synthesis of Digital Systems
ISBN: 0201618605
2. Author: Samir Palnitkar
Title: Verilog HDL
ISBN: 0132599708
3. Author: Blaine Readler
Title: Verilog by Example - A Concise Introduction for FPGA Design
ISBN: 9780983497301

Announcements, course material and other useful links

Will be posted on Blackboard Learn (<http://learn.bu.edu>)

- EC551/Fall 2016

Goals

To provide students with:

- An experience of how to write HDL models that can be automatically synthesized into integrated circuits using programmable hardware such as FPGAs.
- An understanding of how to take an electronic design from concept to register transfer level (RTL) verification and synthesis to final programmable device implementation.
- An experience in writing HDL models of combinational and sequential circuits, synthesizing models, performing simulation, writing test modules, and fitting designs within resource, power, and timing constraints of an FPGA by using automatic place and route CAD software.

Course Outcomes

As an outcome of completing this course, students should be able to:

- Understand advanced topics in digital logic design
- Understand proven design methodologies based on standard EDA tools
- Understand the differences and similarities in hardware and software design
- Understand modern specification methods (HDL)

- Design combinational devices with a full set of EDAtools (skills)
- Understand modeling and verification with hardware description languages
- Understand synthesis with HDLs
- Understand programmable logic devices and FPGAs
- Design state machines, datapath controllers, and assorted CPUs with a full set of EDA tools
- Understand timing analysis
- Understand fault simulation and testing

Evaluation

Midterm – 10%

Final Exam – 10%

Final Project – 40%

Labs (3) – 30%; (10%, 10%, 10%)

Five Homework Assignments – 10% (2% each)

Class participation will help your grade if you are on the border of a grade (e.g. B+ to A-). Class participation includes but is not limited to answering questions in class, attending offices hours, helping others when appropriate in the lab, and serving in a leadership role in your project group.

Homework

Homework assignments will be posted on the Blackboard website **two or more weeks ahead of their due dates**. Homework is to be submitted outside of PHO 336 or in class **before** the beginning of the lecture (**4:05 pm sharp**) on the date specified. You can discuss your work **in the abstract** with other students in the class, but you **must** write-up the solutions on your own.

Labs

Lab descriptions will be posted on the Blackboard website **two or more weeks ahead of their due dates**. Lab assignments are done in groups of **two students**. **Labs are due via Blackboard Learn at 11:59pm on the due date**. You may remain in the same group for the whole semester or change groups with each lab. This is up to you. **Any partner conflicts should be reported EARLY to Prof. Li**.

Exams

There will be one midterm exam and a final exam. **The midterm will be 4-6 pm in class. If you are unable to attend this date, you must provide 1 week advance notice along with appropriate documentation**. The final exam will be **December 20, 3-5 pm in KCB 106**. Make up exams will only be given under extreme circumstances.

Project

Projects will be done in groups of four students (three and five person groups will be allowed in extreme circumstances). **The project will represent a SIGNIFICANT amount of work and will culminate in a demonstrable digital system running on an FPGA**. There will be three project presentations and one

demo session. The first two will be 10 minute, in class updates. **Final project presentations will be during the last week's classes and all team members must be present (see schedule).** Project presentations will be done in front of all students and should be treated as a professional presentation. More information regarding the projects will be provided during the semester. The project demo will be **December 12 (last day of classes), 5-7 pm in PHO 115.** Arrangement for the schedule and process of project demos will be made available later in the semester.

Previous project videos can be found at:

<https://www.youtube.com/channel/UCPYhfQIY30ftfEg7LpRPQtw>

Course Policy

- Homework/Lab: The homework assignments must be the result of your individual work (HW) or you and your partner (labs).
- You may discuss the contents and general approach to a problem with your classmates but not the detailed solution. You are expected to formulate your approach and to write the solutions of HW/Lab problems by yourself/group. Copying the solution and/or answer from another student is considered cheating. Two identical HWs/Labs with same mistakes are considered cheating. **No extensions on homework or labs will be provided. If you will be absent on a day they are due you should make arrangement in advance with Prof. Li.**
- Makeup exams: Makeup exams will be provided if the student receives **prior permission** from the instructor. Emergencies will be dealt on a case-by-case basis. Note that oversleeping, being not ready, or overload due to projects or coursework in other classes are **not** valid excuses for requesting a makeup exam.
- Exam/Home/Lab Grade discussion: Grade discussion/corrections should be done within one week after the graded exam of homework is distributed. **No grade changes will be made after one week, or after the last day of class.**
- I and W grades: As per University policy.
- Honor Code: If you are found cheating on HWs, labs, or examinations, you will be brought up on charges before the Student Academic Conduct Committee whose punishment may include suspension from the University without the right to transfer credits for courses taken elsewhere.

Schedule for EC551 Fall 2016 - Lectures, Homework, Labs and Exams					
Lecture #	Date	Topic Description	Labs Out/Due	Hw Out	Hw Due
1	9/6 (T)	Course Introduction			
2	9/8 (Th)	EDA – Review of combinational logic		THQ1&2	
3	9/13 (T)	EDA – Review of sequential logic			
4	9/15 (Th)	EDA – Quiz review and grading			THQ1&2
5	9/20 (T)	Verilog – Structural and Behavioral Verilog	Prelab	HW1	
6	9/22 (Th)	RC – FPGAs + Paper 1 Out			
7	9/27 (T)	Verilog – Simulation and Test			
8	9/29 (Th)	EDA – Synthesis – Logic Minimization	Lab1/Prelab	HW2	
9	10/4 (T)	Verilog + RC – Guest lecture on Transaction-Level Verilog			HW1
10	10/6 (Th)	Project – Plan and Goals Presentations + Paper 2 Out			
	10/11 (T)	No class (Monday Schedule of Class)			
11	10/13 (Th)	EDA – Sequential Synthesis – Retiming			
12	10/18 (T)	EDA – Paper 1 Discussion + Midterm Review			
13	10/20 (Th)	Midterm (in class)	/Lab1 (due Fri)		
14	10/25 (T)	EDA – Synthesis – Scheduling/Control		HW3	HW2
15	10/27 (Th)	RC – Systolic Arrays	Lab2 (Fri)		
16	11/1 (T)	RC – Guest Lecture + Prior Project Presentations			
17	11/3 (Th)	EDA – Static Timing Analysis			
18	11/8 (T)	Project – Review and Update Presentations		HW4	HW3
19	11/10 (Th)	RC – Paper Discussion 2 + Paper 4 Out			
20	11/15 (T)	EDA – Fault Detection and Diagnosis	Lab3/Lab2 (Mon)		
21	11/17 (Th)	RC – Paper Discussion 3			
22	11/22 (T)	EDA – Formal Verification		HW5	HW4
		Thanksgiving Recess			
23	11/29 (T)	EDA – Physical Design	/Lab3 (Wed)		
24	12/1 (Th)	RC – Paper Discussion 4			
25	12/6 (T)	Project – Final Presentations 1	Project Group1		HW5
26	12/8 (Th)	Project – Final Presentations 2	Project Group2		
	12/12 (M)	Project – Demos, 5-7pm in PHO 115			
	12/20 (T)	Final Exam – 3-5pm in KCB 106			